

# Accelerate<sup>®</sup> - SPB209A EVB- User Guide

## Using PCM interface in Bluetooth

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## 1 PCM Modes of Operation

The PCM interface supports 2 modes of operation

- PCM Master
- PCM Slave

When in PCM master mode, the interface generates a 2MHz or a 2.048 MHz PCM\_CLK and 8kHz PCM\_SYNC signal.

When in PCM slave mode, the interface has both PCM\_CLK and PCM\_SYNC as inputs, thereby letting another unit on the PCM bus generate the signals.

The PCM interface consists of up to 4 PCM slots (time divided) preceded by a PCM sync signal. Each PCM slot can be either 8 or 16 bits wide. The slots can be separated in time, but are not required to follow immediately after 1 other. The timing is relative to PCM\_CLK.

Following is an example of a PCM burst with 2 slots:

The burst starts with a PCM\_SYNC and then follows the PCM burst. Using PCM\_LINK\_SETTINGS command the PCM slots can be configured to start at an arbitrary point of in time, and the start value is given relative to the start of the PCM\_SYNC. Also the start value relative to PCM\_SYNC will vary depending on the Long frame Sync and Short Frame Sync

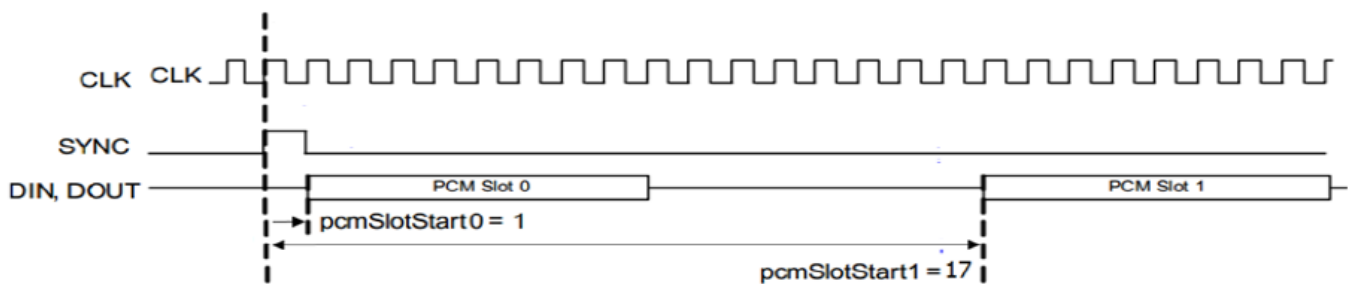
In this example PCM burst consists of 2 PCM slots. PCM settings configured for Short Frame Sync.

The PCM Link Settings for 1<sup>st</sup> PCM Burst – 0x004

- PCM Logical Slot = 0
- PCM Start Slot = 1
- 

The PCM link settings for 2<sup>nd</sup> PCM burst – 0x0045

- PCM Logical Slot = 1
- PCM Start Slot = 17 (0x11)

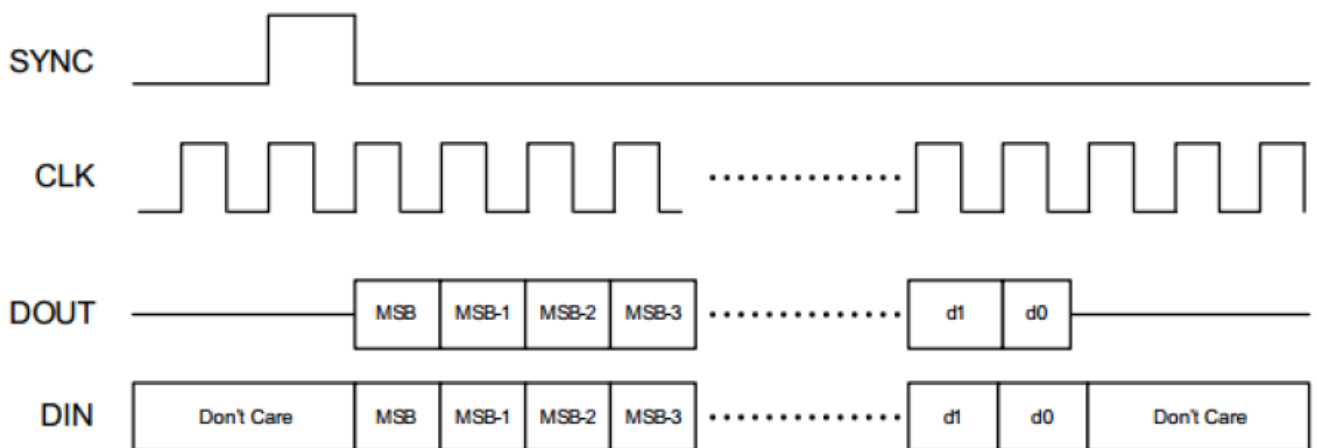


## 2 PCM Protocol Description

The PCM interface supports long frame sync and short frame sync. The pulse width for both long frame sync and short frame sync is 1 bit clock wide.

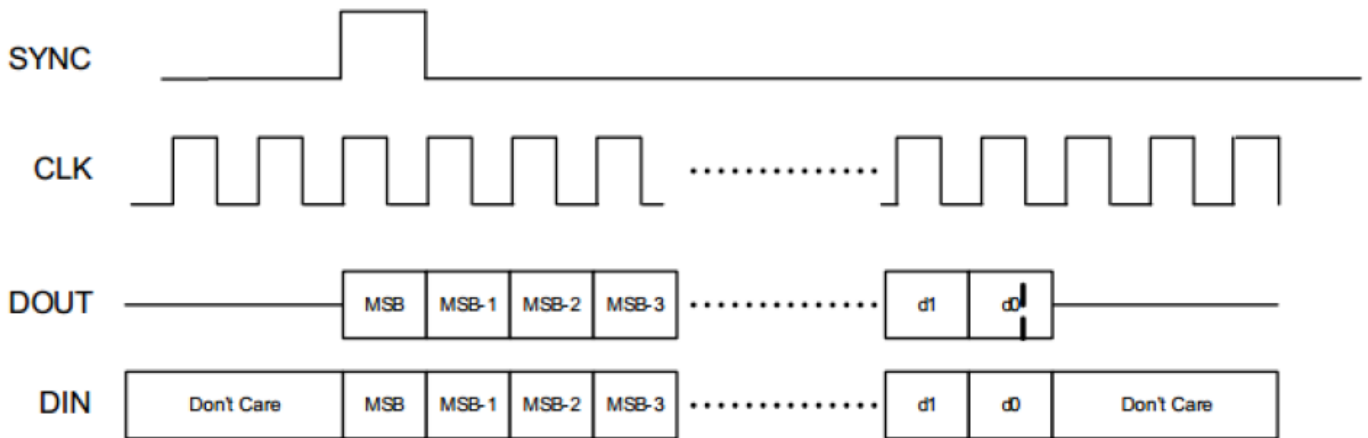
### 2.1 Short Frame Sync

The short frame sync pulse is one clock wide pulse and one clock ahead of first data bit.



### 2.2 Long Frame Sync

The long frame sync pulse is one clock wide pulse and is aligned with first data bit.



### 3 Set-up of PCM interface for Bluetooth operation

The `hcitool` is an operating system tool included in BlueZ (official Linux Bluetooth protocol stack), and is used to configure Bluetooth connections and send special commands to Bluetooth devices. This tool can be used to set-up the SPB209A to operate PCM interface either by manual commands or run a script. The PCM interface utilize defined GPIO:s, see SPB209A datasheet or Hardware Design Guide.

1. Connect the SPB209A EVB to the SDIO slot of the HOST platform. Discover the `hciX` location of the SPB209A with:

```
$ hcitool dev
```

Command shall response with a device ID (below ID is just an example).

```
$ devices:
    hci0    00:11:95:00:1A:CF
```

2. Connect to the SPB209A using `hcitool` and verify connection.

```
$ hcitool cc 00:11:95:00:1A:CF
$ hcitool con
```

3. Configure SPB209A for standard data paths (ACL, SCO/eSCO) as per below choice:

- ACL over Host Interface, see section 3.1.1
- SCO/eSCO over Host Interface (NBS), see section 3.1.2
- SCO/eSCO over PCM Interface (NBS), see section 3.1.3
- SCO/eSCO over PCM Interface (WBS), see section 3.1.4

The set-up is done by HCI commands and a typical HCI command usage format for BlueZ stack on Linux is as follows:

```
$ hcitool cmd <ogf> <ocf> <Parameter>
```

OGF and OCF are the opcodes for the vendor specific commands.

BT Vendor Specific Commands:

- OGF (6 bits) = 0x3F
- OCF (10 bits) = 0x01 -0x80
- PCM/SCO Set-up Commands

## 3.1 Detailed set-up of standard data path

### 3.1.1 ACL over Host Interface

SBC is done from Host and send over HIF. No special configuration is required.

1. Discover the End points of Remote Device
2. Query the capability, configure the Remote Device as below
  - a. Recover Type and Window Size
  - b. Coded Parameters – sampling frequency, channel mode, block length Subbands, allocation method, min bitpool, max bitpool.
  - c. Content Protection method
  - d. Header compression
  - e. Multiplexing Service
3. Open the stream
4. Start the stream (suspend or resume stream after this step)

### 3.1.2 SCO/eSCO over Host Interface (NBS)

1. The hstest application is used for HSP profile from BlueZ. The linux applications such as “mpg123” and “sox” are also required to perform this test.
2. Set-up Host Interface

```
$ hcitool -i hci0 cmd 0x3F 0x1D 0x00
```

3. Set Voice Settings

```
$ hcitool -i hci0 cmd 0x3F 0x26 0x60 0x00
```

4. Put the headset in pairing Mode, Scan from SPB209A to determine the headsets BD address
5. Run “mpg123 -Z -q -s /root/001.mp3 | sox -f raw -r 44100 -c 2 -s -w - -t raw -r 8000 -c 1 -s -w - | hstest play - <BD Address> 1”
6. Enter pin code if required
7. Headset device should hear the music with 001.mp3 played from Host.
8. Stop the test by kill the hstest app and disconnect BR/EDR link

### 3.1.3 SCO/eSCO over PCM Interface (NBS)

1. Voice Path to PCM

```
$ hcitool cmd 3F 1D 01
```

2a. PCM sync settings (PCM I/F Master)

```
$ hcitool cmd 3F 28 03 00 03
```

2b. PCM sync settings (PCM I/F Slave)

```
$ hcitool cmd 3F 28 03 00 00
```

3. PCM link settings

```
$ hcitool cmd 3F 29 04 00
```

4a. PCM settings (PCM I/F Master)

```
$ hcitool cmd 3F 07 02
```

4b. PCM settings (PCM I/F Slave)

```
$ hcitool cmd 3F 07 00
```

5. Pair with Remote Device and create connection

6. Set-up SCO/eSCO Connection with Remote Device

**Note- The PCM settings command need to be issued after every HCI reset command.**

### 3.1.4 SCO/eSCO over PCM Interface (WBS)

1. Voice Path to PCM

```
$ hcitool cmd 3F 1D 01
```

2a. PCM sync settings (PCM I/F Master)

```
$ hcitool cmd 3F 28 03 00 03
```

2b. PCM sync settings (PCM I/F Slave)

```
$ hcitool cmd 3F 28 03 00 00
```

3. PCM link settings

```
$ hcitool cmd 3F 29 04 00
```

4a. PCM settings (PCM I/F Master)

```
$ hcitool cmd 3F 07 02
```

4b. PCM settings (PCM I/F Slave)

```
$ hcitool cmd 3F 07 00
```

5. Enable WBS switch on DUT using following command

```
$ hcitool -i hci0 cmd 0x3F 0x73 0x01
```

6. Create ACL connection with Remote Device

7. Set-up eSCO Connection- using the set-up Synchronous Connection Command

**Note- The PCM settings command need to be issued after every HCI reset command.**

## 3.2 Details of vendor specific command parameters

### 3.2.1 Set SCO Data Path (OCF 0x001D / OGF 0x3F)

The Voice Path command helps to choose between PCM and Host. Default value is 1, corresponding to PCM path. If Audio data path is changed from Host to PCM, ensure that this is the first command to be issued, before any other PCM command.

Name	Length	Description
Voice Path	1	0x00 = Host 0x01 = PCM

[Default command : hcitool cmd 0x3f 0x1D 0x01]

### 3.2.2 Write PCM Synchronous Settings (OCF 0x0028 / OGF 0x3F)

The PCM sync setting command is used to configure PCM Sync Format, short Sync and Long Sync; Set PCM Sync frequency to 8 kHz or 16 kHz, Voice data control settings when voice is configured over Host interface.

The following are applicable for the PCM Synchronous Settings command:

Name	Length	Description
PCM Sync Settings 1	1	Default = 0x03
PCM Sync Settings 2	2	Default = 0x0000

[Default command : hcitool cmd 0x3f 0x28 0x03 0x00 0x00]

- First byte PCM Synchronous Settings 1
  - PCM Synchronous Settings 1, Bit[0]: Used only for voice over host interface  
Controls how voice samples are moved between memory and receive/transmit buffers in hardware. It is recommended to leave this bit to 1 for optimal performance.  
ISR (IramSyncRate) only valid if IF = Host  
Bit[0] = 0 = burst mode, controlled by reception and transmission of voice packets  
Bit[0] = 1 = fixed rate mode of 8k samples/s (better audio quality, hence default)
  - PCM Synchronous Settings 1, Bit[1]: Used only for voice over host interface  
It is recommended to leave this bit to 1 for optimal performance.  
ISS (IramSync Source) only valid if IF = Host and ISR = Fixed Rate

Bit[0] = 0 = ISR is not aligned to frame tick

Bit[0] = 1 = ISR is aligned to frame tick

- Next 2 bytes are 16-bit value PCM Synchronous Settings 2
  - PCM Synchronous Settings 2, Bits[1:0]: *pcmlfMode*  
00 = PCM short synchronous mode  
01 = PCM long synchronous mode
  - PCM Synchronous Settings 2, Bit[8];  
Bit[8] = 0 = disable PCM *mclk* generation  
Bit[8] = 1 = enable PCM *mclk* generation
  - PCM Synchronous Settings 2, Bit[9]:  
Bit[9] = 0 = default  
Bit[9] = 1 = selects 2.048 MHz clock for PCM *mclk*
  - PCM Synchronous Settings 2, Bit[10]  
Used in WB speech feature in which the PCM interface is 16 kHz with 16-bit PCM data  
0 = PCM Sync is 8 kHz  
1 = PCM Sync is 16 kHz

### 3.2.3 Write PCM Link Settings (OCF 0x0029 / OGF 0x3F)

The following are applicable for PCM Link Settings command:

Name	Length	Description
PCM Link Settings	2	Default: 0x0004 = first SCO link 0x0045 = second SCO link 0x0086 = third SCO link

- Write PCM Link Settings, Bits[1:0]: Choose the PCM slot to use (only one slot supported)
  - Bits[1:0] = 00 = slot 0
  - Bits[1:0] = 01 = slot 1
  - Bits[1:0] = 10 = slot 2
  - Bits[1:0] = 11 = slot 3
- Write PCM Link Settings, Bits[9:2]: Choose the PCM slot start
- Write PCM Link Settings, Bits[13:10]: Disable PCM out, bit mask
- Default value as 0x0004 for first SCO link:
  - PCM Logical Slot = 0
  - PCM Start Slot = 1
  - PCM Disable = 0
- Default value as 0x0045 for second SCO link:
  - PCM Logical Slot = 1
  - PCM Start Slot = 17 (0x11)
  - PCM Disable = 0
- Default value as 0x0086 for third SCO link:
  - PCM Logical Slot = 2
  - PCM start Slot = 33 (0x21)
  - PCM Disable = 0

Note – this command should be issued before setting up each of the SCO links to control the PCM slots for links.

### 3.2.4 Write PCM settings (OCF 0x0007 / OGF 0x3F)

The following are applicable for the PCM Settings command:

Name	Length	Description
PCM Settings	1	Default: 0x02

- Choose TX and RX as Port A or B
  - Bit[0]: PCM Direction  
0 = port A receive, port B transmit  
1 = port A transmit, port B receive
- Master or Slave settings
  - Bit[1]: Master/Slave  
0 = PCM I/F slave, external PCM clock and synchronization  
1 = PCM I/F master, internal PCM clock and synchronization
- PCM synchronous generated from frame tick or system clock tick
  - Bit[2]: PCM Sync Source  
0 = PCM sync page generated from system clock  
1 = PCM sync page generated from frame clock
- Bit[3]: Reserved
- Enable PCM pull-up after tri-state, recommended if there are multiple PCM devices on the host PCM bus and Bluetooth is in Deep Sleep state. The PCM clock is normally terminated after the last data bit has been transmitted. Selection can be done to make the PCM clock to be available continuously
  - Bit[4]: PCM Clock On  
0 = PCM clock is terminated after last data bit has been transmitted  
1 = Make PCM clock available continuously

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