Hardware Design Guide
SPB209A
Application Note

1 Preface

This document provides hardware design guidelines for the SPB209A module.

2 Introduction

2.1 Overview

SPB209A is a complete WLAN/BT/NFC module with EMC shield, ready for onboard integration in a hosted environment. SPB209A enables a cost efficient ultra-low power, high performance and feature rich client solution. It provides up to 433 Mbit/s data rate when operating in the OFDM mode and up to 11 Mbit/s data rate when operating in the DSSS/CCK mode.

SPB209A integrates RF, baseband/MAC, Bluetooth Package Engine, NFC, memory, RF filters, oscillator, antenna (option) and EMC shield into a highly integrated and optimized module solution with high quality and reliability to a complete standalone solution with no need for external components.

This highly integrated solution is optimized for customer applications running on a Linux host. The host interface supports SDIO 3.0 and High Speed UART. Internal RAM comprises both code and data memory eliminating the need for external RAM, Flash or ROM memory interfaces. MAC address, trimming values etc. are stored in the on board memory.

2.2 Key Features

- Support for 802.11a/b/g/n/ac
- Data Rates: 20MHz channel bandwidth: 1-86Mbps; 40MHz channel bandwidth: 13-200Mbps; 80MHz channel bandwidth: 29-433Mbps
- Modulation: BPSK, CCK, QPSK, 16QAM, 64QAM 256 QAM for WLAN and GFSK/π/4DQPSK/8DPSK/LE for BT
- Open WEP, WPA/WPA2 encryption
- No external components except for the antenna options
- Low power consumption due to efficient PA design and power off mode
- An on-board 32 kHz oscillator maintains real time in power save mode, allows the high frequency clock to be turned off.
- Supports BT-WLAN coexistence.
- Extensive DMA hardware support for data flow to reduce CPU load.
- Advanced power management for optimum power consumption at varying load.
- External interfaces 4 bit SDIO 3.0 for WLAN/BT or UART/PCM for BT interface.
- On-board High Frequency High Precision Oscillator 37.4 MHz
- Small footprint 14 x 14 mm (196 mm2) 41-pin
- RoHS Compliant

3 Block Diagram

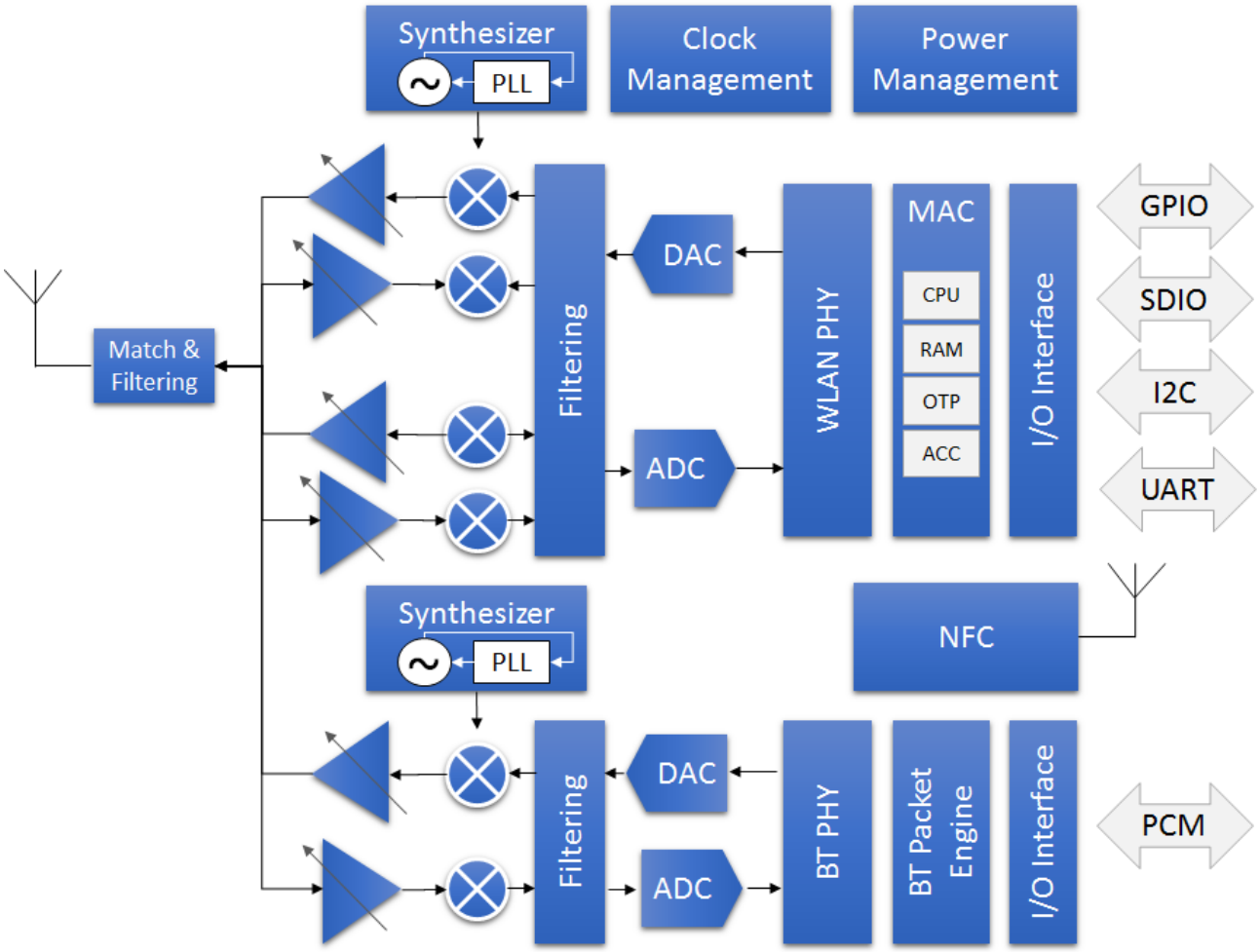

Figure 1. Block diagram.

4 Reference schematic

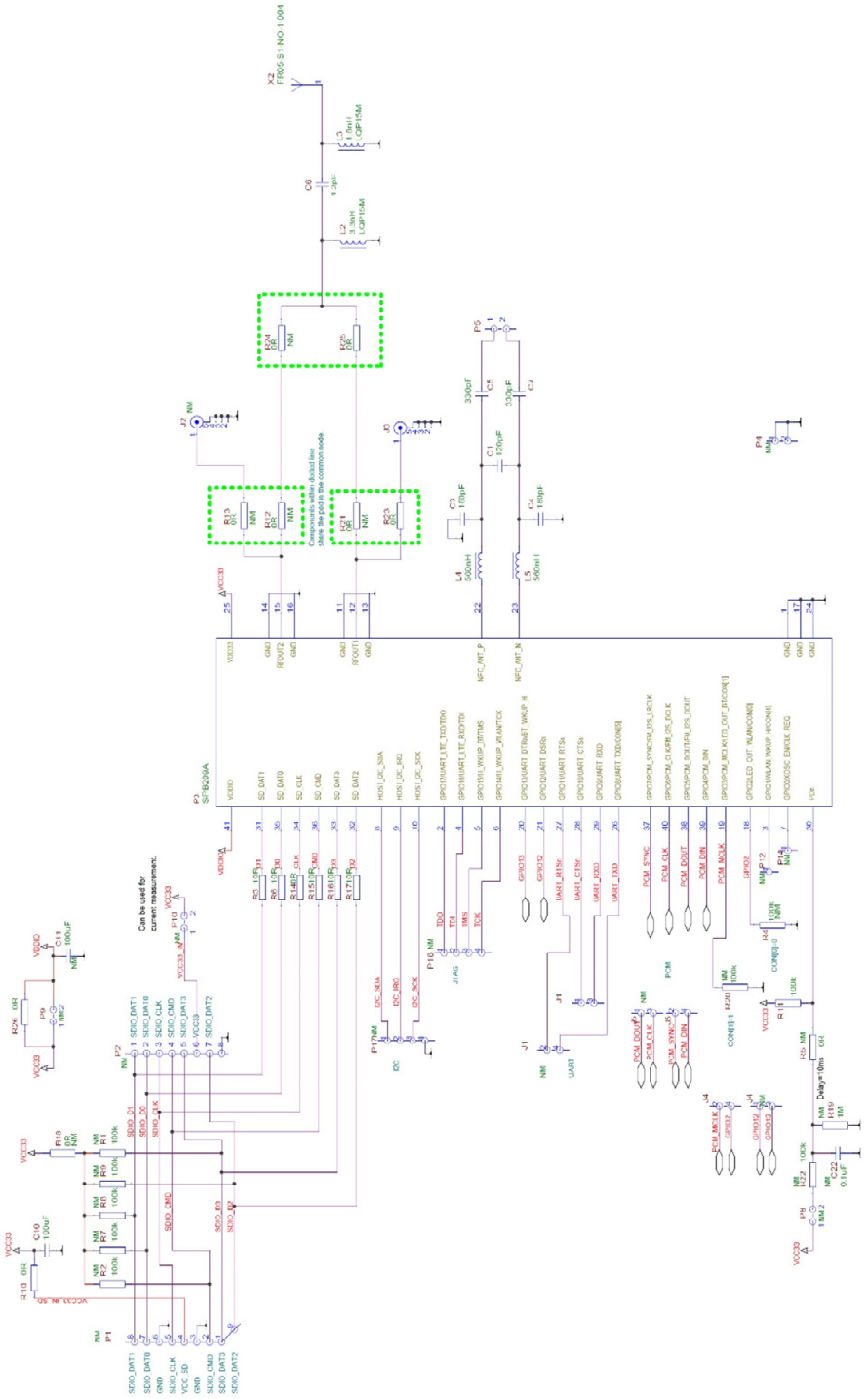

Figure 2. SPB209A reference schematic.
Note that the module has two RF output options, and one of them is used depending on the version ordered. The reference schematic is made so both versions can be used and have access to the single common antenna by means of mounting selected 0R resistors on the output.

5 Pin Description

The SPB209A module provides a number of multi-function IOs that are software configurable.

Table 1. RF Interface

Module Pin number	Pin Name	Description
12	RFOUT1	RF input/output (default)
15	RFOUT2	RF input/output (available on customer special request, contact sales for this option)

Table 2. NFC Interface

Module Pin number	Pin Name	Description
22	NFC_ANT_P	NFC antenna interface, positive
23	NFC_ANT_N	NFC antenna interface, negative

Table 3. SDIO Host Interface

Module Pin number	Pin Name	Description
34	SD_CLK	Clock input
36	SD_CMD	SDIO 4-bit mode: Command SDIO 1-bit mode: Command
33	SD_DAT3	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used
32	SD_DAT2	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
31	SD_DAT1	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt
35	SD_DAT0	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line

The SDIO Interface supports 1-bit and 4-bit SDIO transfer modes up to 208MHz clock frequency.

Table 4. I2C Compatible Host Interface (slave)

Module Pin number	Pin Name	Description
8	HOST_I2C_SDA	Serial data
9	HOST_I2C_IRQ	Interrupt to host from slave
10	HOST_I2C_SCK	Serial clock

The I2C interface is currently not supported.

Table 5. Multi-Purpose Interface[1]

Pin number	Pin Name	No Pad Power State	Reset State	HW[2] State	PD[3] State	PD[4] Prog	Internal PU/PD	PU[5]	PD[5]
2	GPIO17	Tristate	Input	Input	Tristate	Yes	Weak PU	No	No
GPIO Mode: GPIO17 (input/output) JTAG Mode: TDO (JTAG test data output) LTE Coexistence Mode: UART_LTE_TXD (output)									
4	GPIO16	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO16 (input/output) JTAG Mode: TDI (JTAG test data input) LTE Coexistence Mode: UART_LTE_RXD (input)									
5	GPIO15	Tristate	Input	Input	Drive high	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO15 input/output) JTAG Mode: TMS (JTAG controller select, input) Out-of-Band Mode: Host wakeup Bluetooth (input)									
6	GPIO14	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO14 (input/output) JTAG Mode: TCK (JTAG test clock, input) Out-of-Band Mode: Host wakeup WLAN (input)									
20	GPIO13	Tristate	Input	Input	Drive high	Yes	Nominal PU	No	No
GPIO Mode: GPIO13 (input/output) UART Mode: UART_DTRn (output) Out-of-Band Mode: Bluetooth wakeup host (output)									
21	GPIO12	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO12 (input/output) UART Mode: UART_DSRn (input)									
27	GPIO11	Tristate	Input	Input	Drive high	Yes	Weak PU	No	No
GPIO Mode: GPIO11 (input/output) UART Mode: UART_RTSn (output)									
28	GPIO10	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO10 (input/output) UART Mode: UART_CTSn (input)									
29	GPIO9	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO9 (input/output) UART Mode: UART_RXD (input)									
26	GPIO8	Tristate	Input	Input	Drive low	Yes	Weak PU	No	No
GPIO Mode: GPIO8 (input/output) UART Mode: UART_TXD (input)									
37	GPIO7	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO7 (input/output) PCM Mode: PCM_SYNC (output if master, input if slave)									
40	GPIO6	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO6 (input/output) PCM Mode: PCM_CLK (output if master/input if slave)									

Pin number	Pin Name	No Pad Power State	Reset State	HW[2] State	PD[3] State	PD[4] Prog	Internal PU/PD	PU[5]	PD[5]
38	GPIO5	Tristate	Input	Input	Tristate	Yes	Weak PU	Yes	Yes
GPIO Mode: GPIO5 (input/output) PCM Mode: PCM_DOUT (output)									
39	GPIO4	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO4 (input/output) PCM Mode: PCM_DIN (input)									
19	GPIO3	Tristate	Input	Output	Tristate	Yes	Weak PU	No	No
GPIO Mode: GPIO3 (input/output) PCM Mode: PCM_MCLK (optional, output if master/input if slave) LED Mode: LED_OUT_BT (output) Configuration Mode: CON[1] (input)									
18	GPIO2	Tristate	Input	Output	Tristate	Yes	Weak PU	No	No
GPIO Mode: GPIO2 (input/output) LED Mode: LED_OUT_WLAN (output) Configuration Mode: CON[0] (input)									
3	GPIO1	Tristate	Input	Input	Tristate	Yes	Weak PU	No	No
GPIO Mode: GPIO1 (input/output) Out-of-Band Mode: WLAN wakeup host (output)									
7	GPIO0	Tristate	Output	Output	Drive low	Yes	Nominal PU	Yes	No
GPIO Mode: GPIO0 (input/output) Oscillator Mode: XOSC_EN/CLK_REQ (output) 0=disable external oscillator 1=enable external oscillator)									
30	PDn	-	-	-	-	-	-	-	-
Full power-down (input) 0 = full power-down 1 = normal mode • Connect to power-down pin of host or VDD33. • External host required to drive this pin high for normal operation. No internal pull-up on this pin.									

(1) Not all GPIO pins can be used for wakeup signals.
(2) Hardware default state after reset.
(3) Power-down state.
(4) Power-down state programmable.
(5) Programmable pull-up/pull-down.

Table 6 Supply Interface

Module Pin number	Pin Name	Description
25	VDD33	Analog 3.3V Supply, decouple with 100uF.
41	VDDIO	Digital IO supply, can be connected with VDD33 and share decoupling.
1,11,13,14, 16,17,24	GND	Ground

6 Firmware Boot Options

GPIO3 (CON[1]) and GPIO2 (CON[0]) serves as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their normal function. To set a configuration bit to 0, attach a 100kohm resistor from the pin to ground. No external circuitry is needed to set a configuration bit to 1. Software reads and boots according to table below.

Table 7 Boot options

CON[1:0]	WLAN	BT/BLE/NFC	FW Download Interface	FW Download Mode	Number of SDIO Functions
00	SDIO	UART	SDIO	Serial	1 (WLAN)
01	SDIO	SDIO	SDIO	Parallel	3 (WLAN, BT, NFC)
10	SDIO	UART	SDIO+UART	Parallel	1 (WLAN)
11 (default)	SDIO	SDIO	SDIO	Serial	3 (WLAN, BT, NFC)

Different boot options requires different firmware drivers. Currently, only the default configuration is supported.

7 Bill of Material

Comp	Part name	MFG nr	Description
A1	PCB		Printed circuit board
C1	120PF 0402 C0G 50V 5% HDW	GRM1555C1H121JA01D	Murata GRM15 Series Chip Monolithic Ceramic Capacitor
C3	180PF 0402 C0G 50V 5% HDW	GRM1555C1H181JA01D	Murata GRM15 Series Chip Monolithic Ceramic Capacitor
C4	180PF 0402 C0G 50V 5% HDW	GRM1555C1H181JA01D	Murata GRM15 Series Chip Monolithic Ceramic Capacitor
C5	330PF 0402 C0G 50V 5% HDW	GRM1555C1H331JA01	Murata GRM15 Series Chip Monolithic Ceramic Capacitor
C6	1.2PF 0402 C0G 50V HDW		Murata GRM15 Series Chip Monolithic Ceramic Capacitor
C7	330PF 0402 C0G 50V 5% HDW	GRM1555C1H331JA01	Murata GRM15 Series Chip Monolithic Ceramic Capacitor
C10	100UF 6.3V X7R 1206 HDW		Ceramic chip capacitor
J3	SMA JACK EDGE MOUNT 132357		Amphenol 132357-11
L2	3N3 0402 0.1NH LQP15M HDW	LQP15MN3N3B02	Murata LQP15MN3N3B02 Film Type Chip Coil
L3	1N8 0402 0.1NH LQP15M HDW	LQP15MN1N8B02	Murata LQP15MN Film Type Chip Coil
L4	560NH 0402 5% LQB15 HDW	LQB15NNR56J10	Murata LQB15NN Film Type Chip Coil
L5	560NH 0402 5% LQB15 HDW	LQB15NNR56J10	Murata LQB15NN Film Type Chip Coil
P3	SPB209A		SPB209A PCB Module
P5	WAFER 2-2.54 HDW		Pin Posts single row C/C 2.54 2-Pin
R3	10R 0402 1% HDW	RC0402FR-0710RL	Chip resistor 0.063W
R6	10R 0402 1% HDW	RC0402FR-0710RL	Chip resistor 0.063W
R10	0R 0402 HDW	RC0402JR-070RL	Chip resistor 0.063W
R11	100K 0402 1% HDW	RC0402FR-07100KL	Chip resistor 0.063W
R14	0R 0402 HDW	RC0402JR-070RL	Chip resistor 0.063W
R15	10R 0402 1% HDW	RC0402FR-0710RL	Chip resistor 0.063W
R16	10R 0402 1% HDW	RC0402FR-0710RL	Chip resistor 0.063W
R17	10R 0402 1% HDW	RC0402FR-0710RL	Chip resistor 0.063W
R23	0R 0402 HDW	RC0402JR-070RL	Chip resistor 0.063W
R25	0R 0402 HDW	RC0402JR-070RL	Chip resistor 0.063W
R26	0R 0402 HDW	RC0402JR-070RL	Chip resistor 0.063W
X2	ANTENNA FR05-S1-NO-1-004 SMD	FR05-S1-NO-1-004	Fractus Dual-band Reach Xtend Chip Antenna

Figure 3. Reference schematic BOM.

8 PCB layout

Use normal layout common sense. Include a pi-network in front of the antenna to add the possibility to tune its impedance to 50ohm. The module requires a 50ohm load on its RF pins. If another antenna is used, the matching components need to be revised. The power supply is arranged as power planes on the bottom layer with vias up to the top level. The four layers of the reference pcb is shown below, where the red area is the VCC33 net and the black is the VDDIO net. All IOs are connected to pin-strips for test purposes.

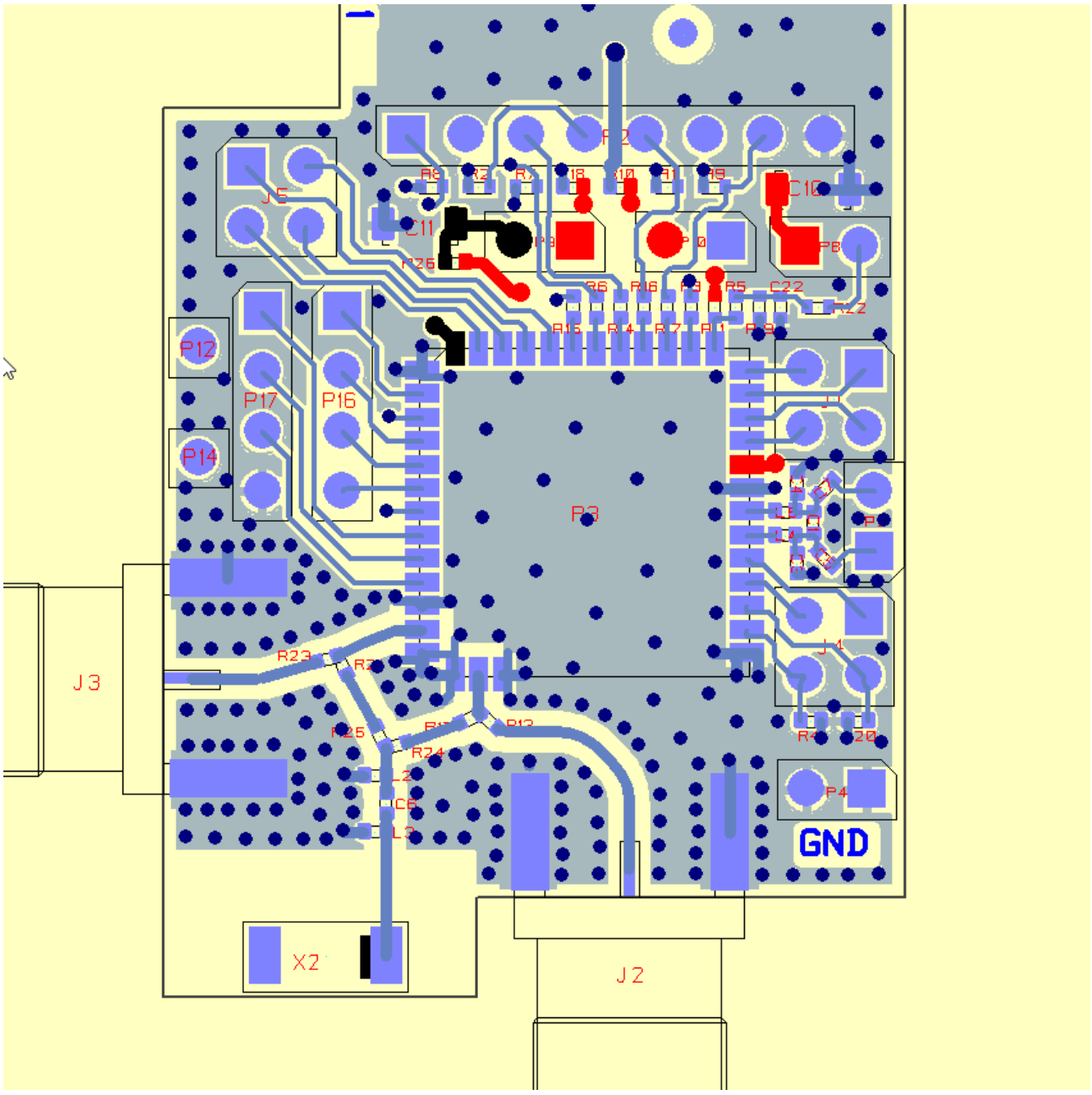

Figure 4. Top layer.

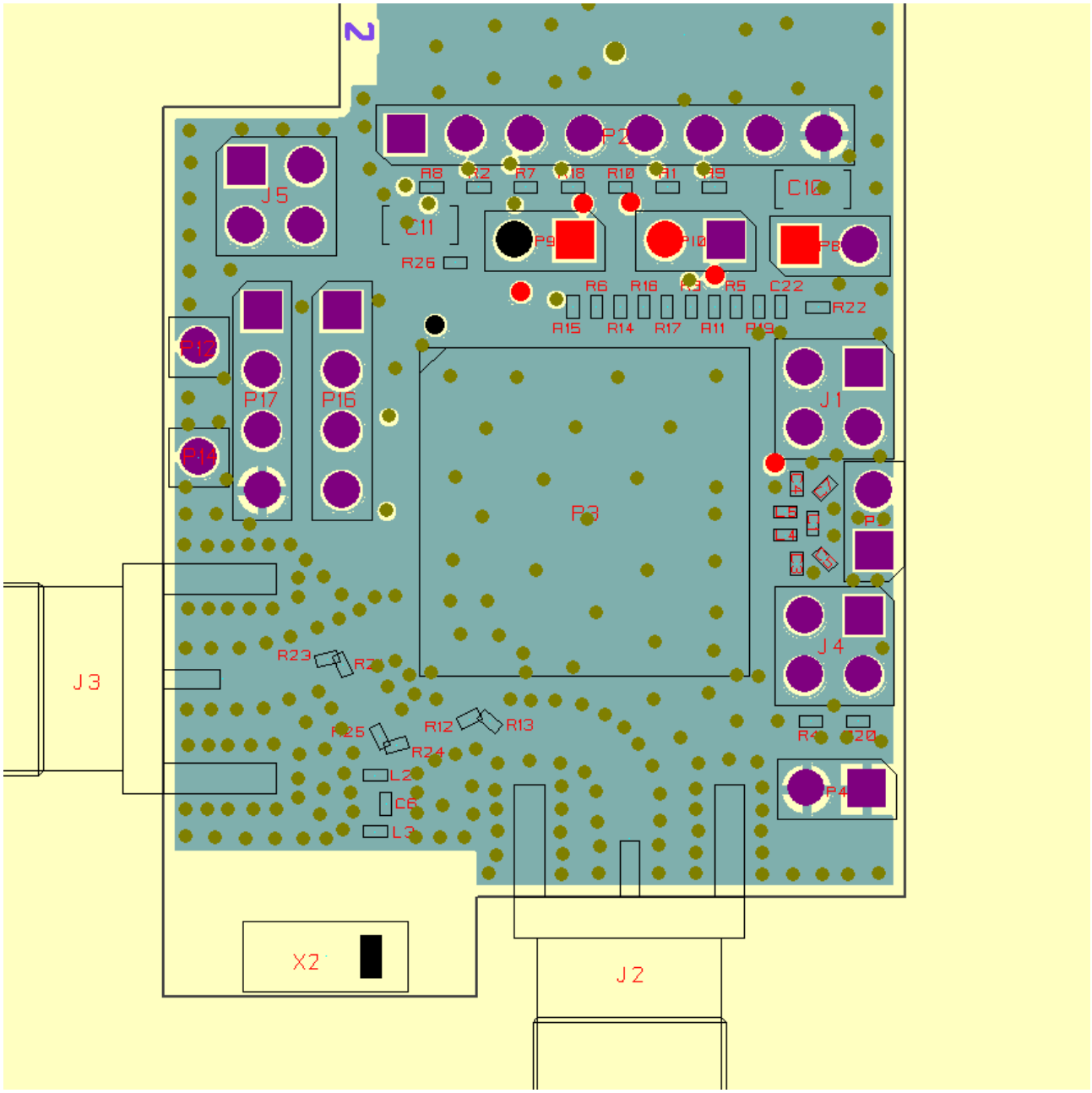

Figure 5. Second layer (RF ground).

Figure 6. Third layer, ground and supply.

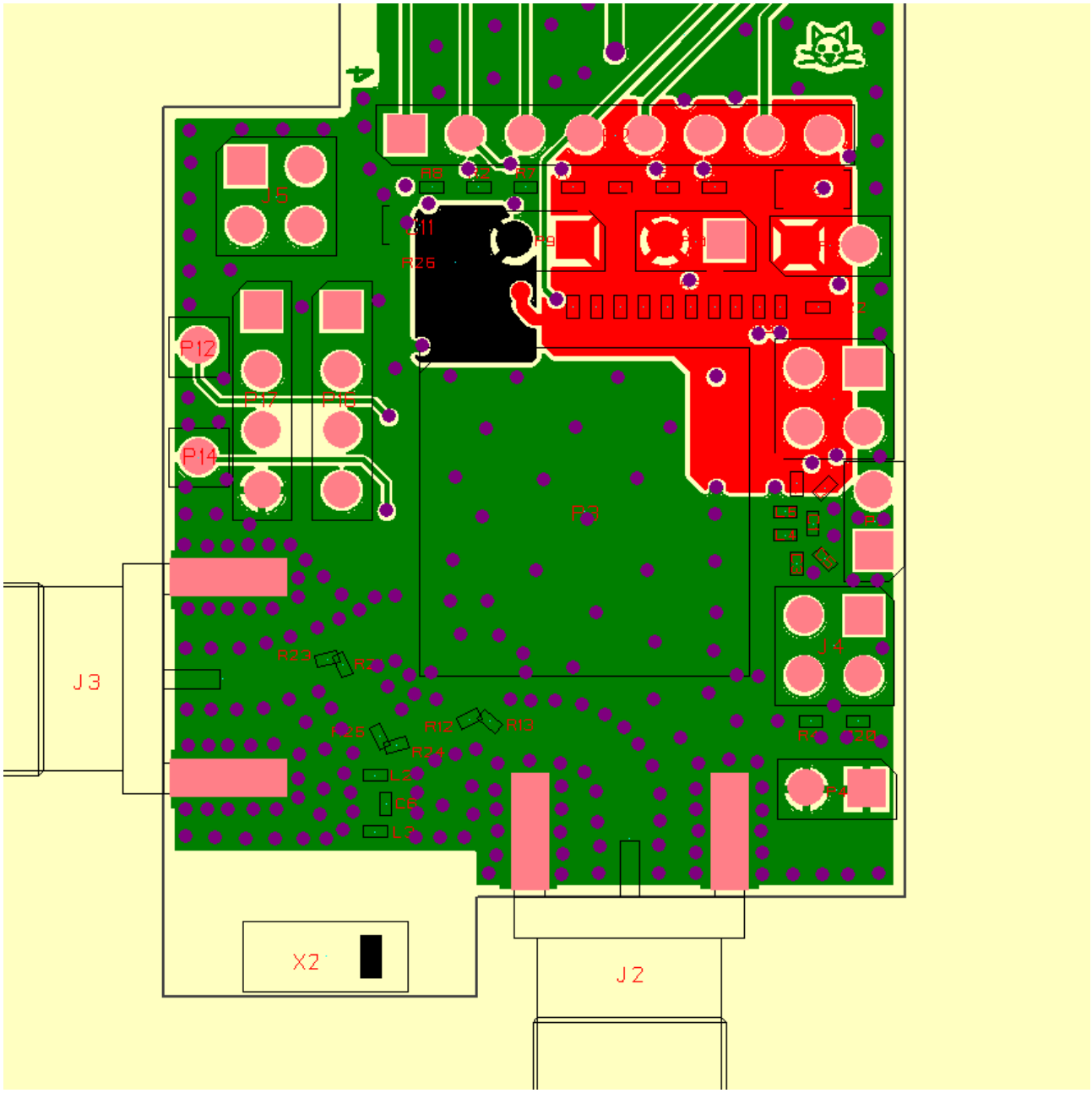

Figure 7. Bottom layer, ground and supply.

9 NFC

An NFC antenna coil may be added as an external component but is not included in the reference design. H&D Wireless has used the ANFCA-4545-A01 coil from Abracon during verification and FCC/ETSI certification. It is connected to pin-strip P5 on the reference board, see Figure 8 below. The NFC output consist of a low-pass filter for harmonics suppression followed by a matching network. The matching network was tuned to have proper operation together with the antenna coil. On a customer board using the same or another NFC antenna coil, it is recommended to overlook the matching component values to ensure proper operation.

C1, C3 and C4 in the reference schematic together with C5, C7 and the antenna inductance should be resonant at 13.56 MHz. Do not change C3/C4 (180pF) as they act as a low pass filter.

If C1 is 120pF, the impedance of C1//(C3+C4) is 210 pF = -j56 ohm.
The antenna inductance + C5 + C7 should then be approximately +j56 ohm.

The antenna inductance in the reference design is 1.5 µH (+j128 ohm). C5 and C7 should then be –j36 ohm each, or 326 pF. 330 pF is the closest value.

The transmitted power can be increased by lowering the series capacitors, C5 and C7. The total impedance of these capacitors and the antenna inductance could typically be as low as +j10 ohm. The capacitors should then be –j59 each, or 200 pF. C1 should then accordingly be 1.1 nF for the circuit to resonate at 13.56 MHz.

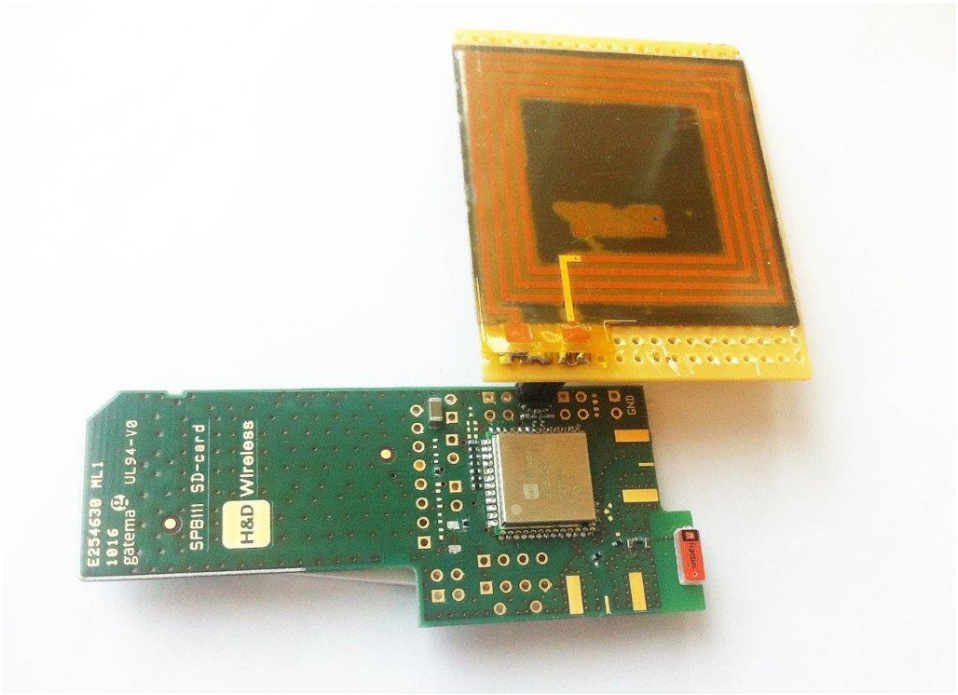

Figure 8. Example of NFC antenna coil mounted on the reference board.

10 Antennas

The antenna used on the SPB111 reference board is the dual band antenna FR05-S1-NO-1-004 from Fractus. It has a peak gain of 1.8dB dBi in the 2.4-2.5GHz band and 4.9dBi in the 4.9-5.875GHz band. The SPB209A modules have been FCC/ETSI certified with this antenna. Should another antenna be used in a customer product, the antenna gain together with the path loss in the product should be kept below the above values in order to avoid adjustments to the SPB209A module. It is always good practice to add pads for a pi-network close to the antenna in the event that it needs to be tuned.

11 Current measurement

Current consumption can be measured by using an external 3.3V supply. This involves removing 0ohm resistor R10 and mounting a single pin strip on connector P10:2 (see Figure 4, red circle) where the external 3.3V should be applied. Ground can be made available by mounting a single pin-strip on either connector P2:8 or a double on connector P4.

12 Package Specifications

12.1 Mechanical outline

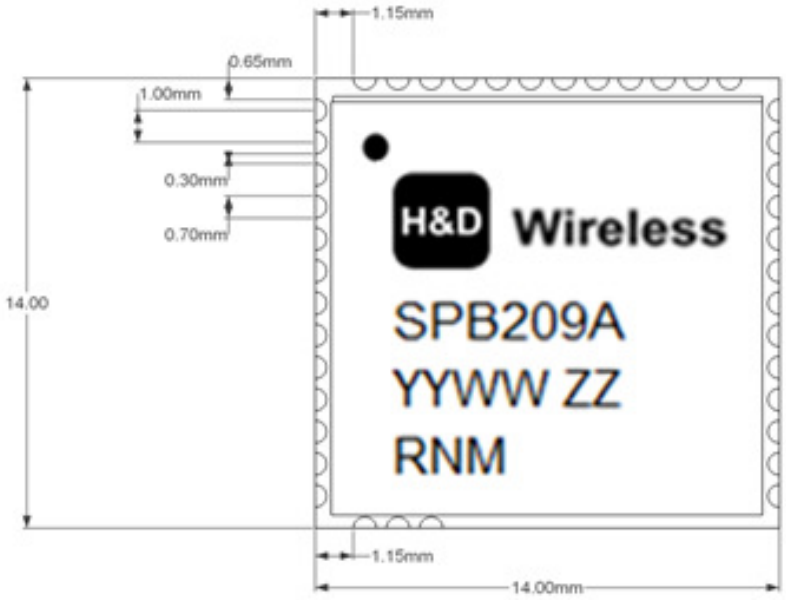

Figure 9. Package dimensions, top view.

Figure 10. Package dimensions, side view.

12.2 Mounting information

Recommended land pattern on the PCB.

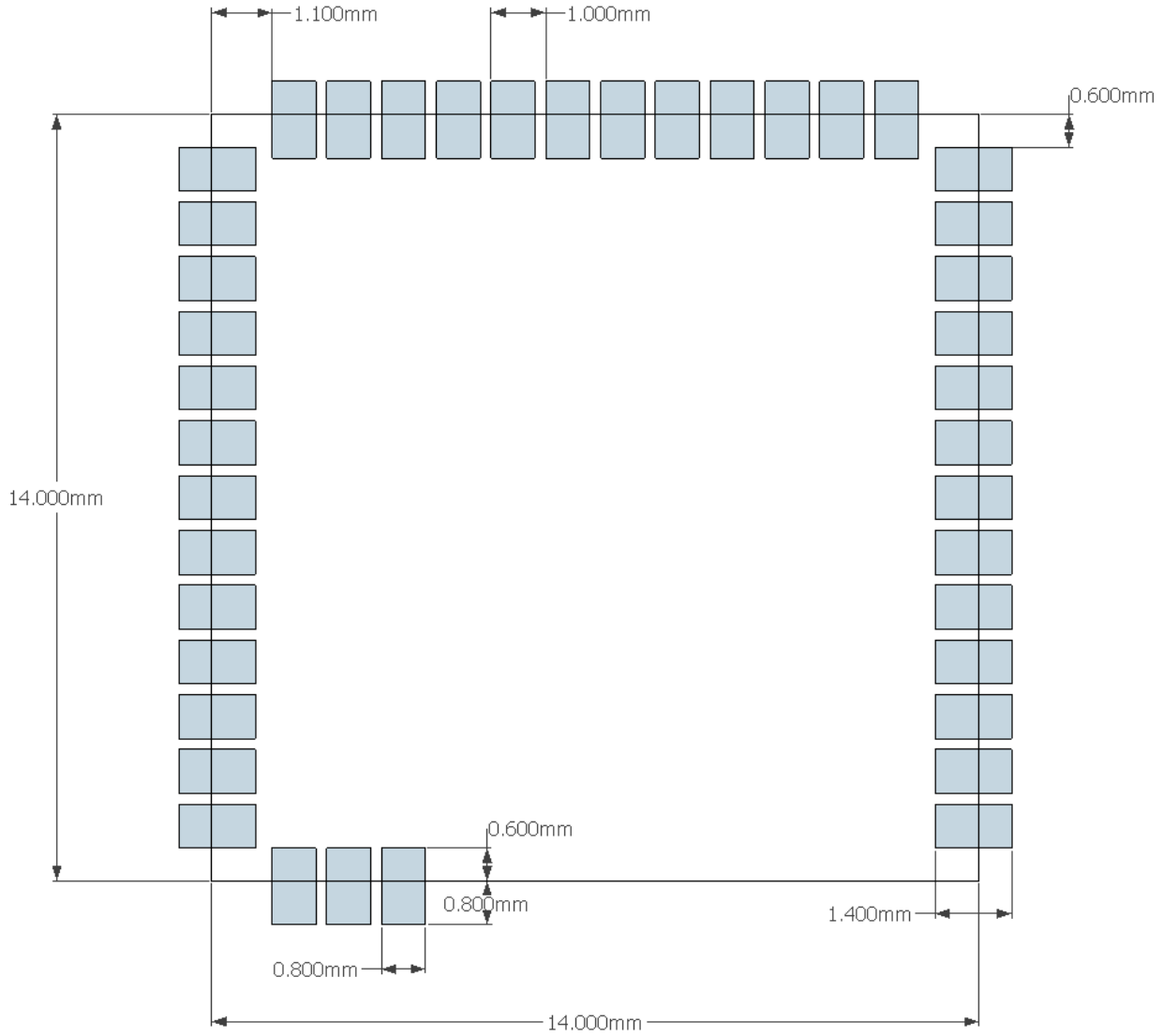

Figure 11. Recommended land pattern on the PCB, top view.

13 Reference PCB Stack-up

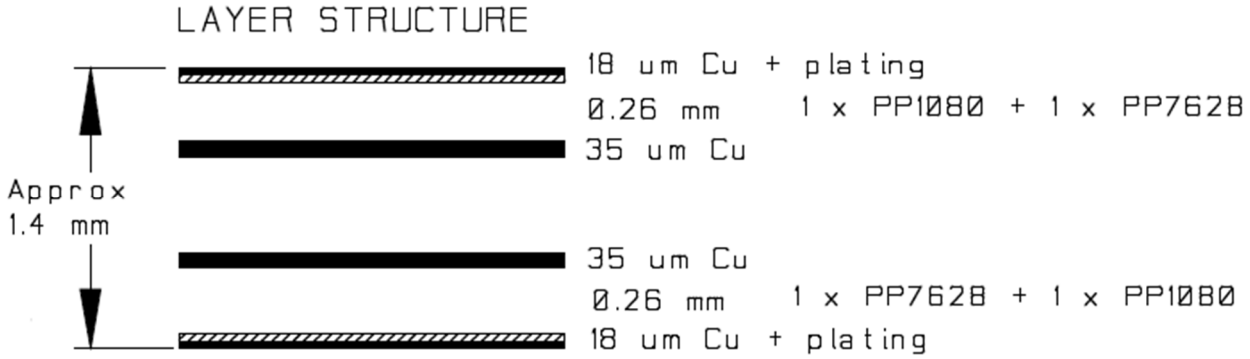

Figure 12. Reference PCB stack-up.