Hardware Design Guide
HDG200 R2A
Application Note

1 Preface

This document provides hardware design guidelines for the HDG200 WLAN SiP revision R2A.

2 Introduction

2.1 Overview

HDG200 is a complete WLAN System In Package, SIP, solution specifically designed to address the proliferation of Wi-Fi technology into embedded devices. HDG200 enables a cost efficient ultra low power, high performance and feature rich client solution. It provides up to 65 Mbit/s data rate when operating in the OFDM mode and up to 11 Mbit/s data rate when operating in the DSSS/CCK mode.

HDG200 integrates RF, baseband/MAC, memory, RF filters and oscillator into a highly integrated and optimized SIP (System In Package) solution with high quality and reliability. This minimizes the need of external components, simplifying assembly and test.

This highly integrated solution is optimized for customer applications running on a host CPU.
The host interface supports SDIO and SPI. Internal RAM comprises both code and data memory eliminating the need for external RAM, Flash or ROM memory interfaces.
MAC address, trimming values etc. are stored in the on board memory.

2.2 Key Features

- Support for 802.11b/g/n
- Data Rates: 1, 2, 5.5, 6, 7.2, 9, 11, 12, 14.4, 18, 21.7, 24, 28.9, 36, 43.3, 48, 54, 57.8, 65 Mbps
- Modulation: QPSK, 16QAM, 64QAM DBPSK, DQPSK, CCK, OFDM with BPSK
- Open WEP, WPA/WPA2 encryption
- No external RF components
- Low power consumption due to efficient PA design
- An internal 32 kHz oscillator maintains real time in power save mode, allows the high frequency clock to be turned off.
- Advanced power management for optimum power consumption at varying load.
- External interfaces SDIO/SPI
- On-board High Frequency High Precision Oscillator 40 MHz
- Wide Range Supply Voltage, 2.85-4.35 V
- Small footprint 8 x 8 mm (64 mm2) 44-pin QFN
- RoHS Compliant

2.3 Block Diagram

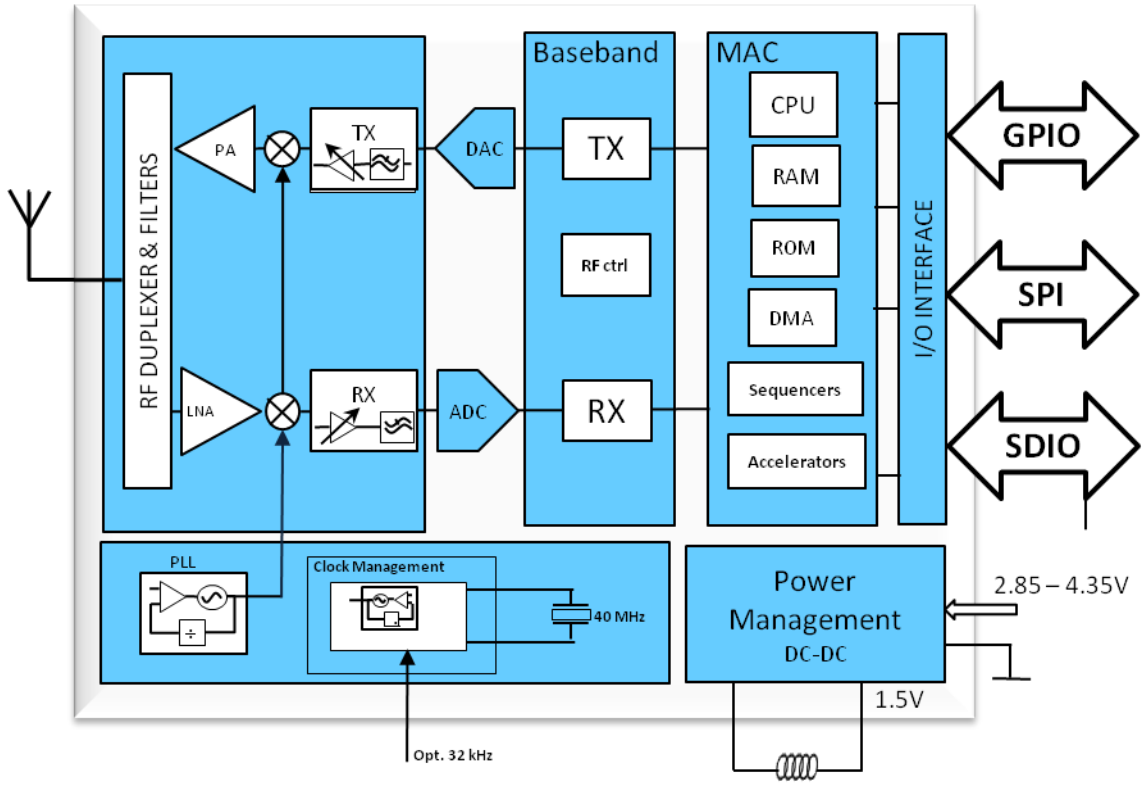

Figure 2-1: Block Diagram

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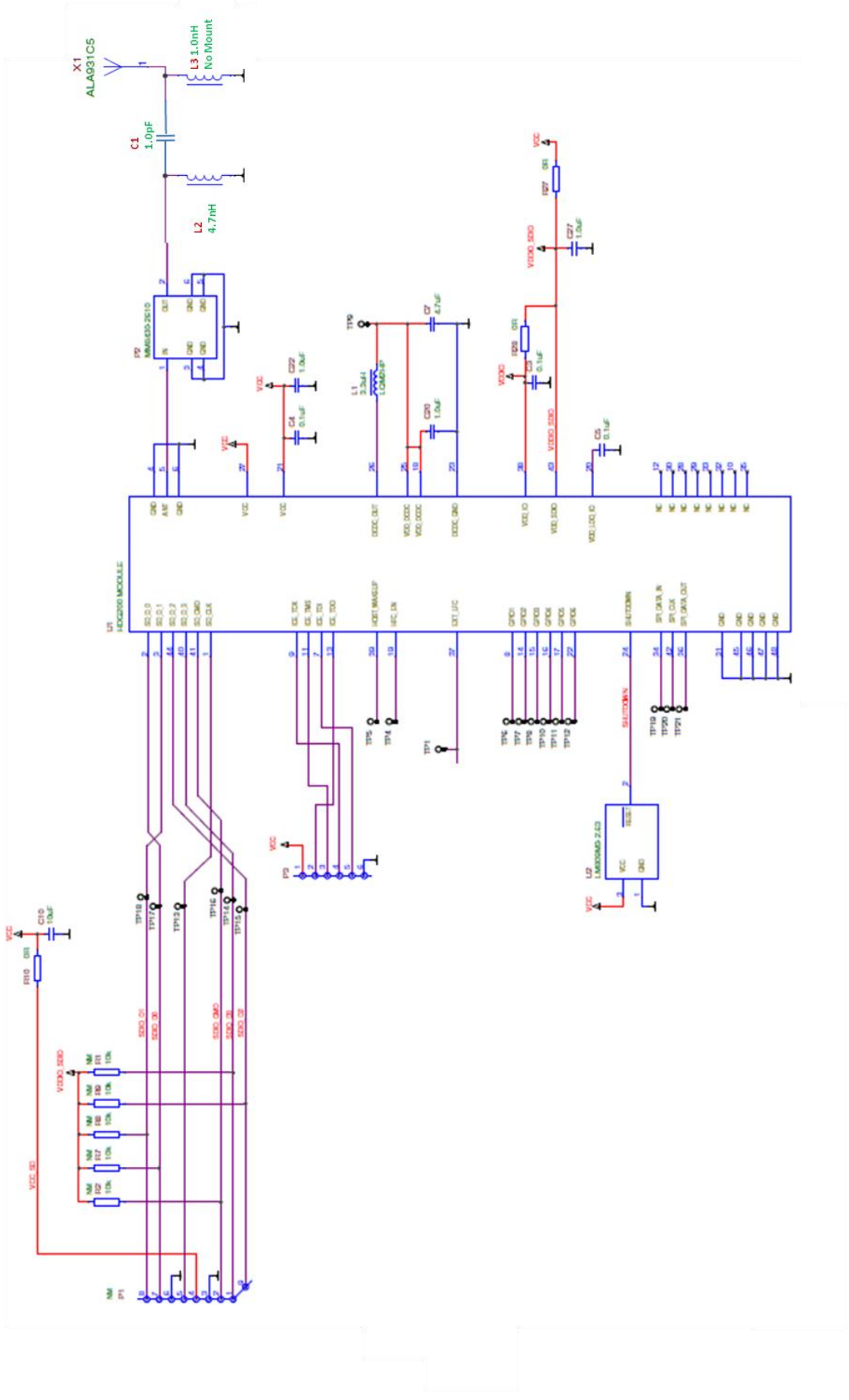
3 Reference schematic



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4 Bill of Material

Comp	Part name	Description
A1	PCB	Printed circuit board
C1	1.0pF 0402 C0G 6.3V	GJM15 Series Chip Monolithic Ceramic Capacitor
C3	0.1UF 0402 X7R 16V	GRM15 Series Chip Monolithic Ceramic Capacitor
C4	0.1UF 0402 X7R 16V	GRM15 Series Chip Monolithic Ceramic Capacitor
C5	0.1UF 0402 X7R 16V	GRM15 Series Chip Monolithic Ceramic Capacitor
C7	4.7UF 0805 X5R 10V	AVX 0805ZD475K 10%
C10	10UF 0805 X5R 10V	GRM21 Series Chip Monolithic Ceramic Capacitor
C20	1.0UF 0402 X5R 6.3V	GRM15 Series Chip Monolithic Ceramic Capacitor
C22	1.0UF 0402 X5R 6.3V	GRM15 Series Chip Monolithic Ceramic Capacitor
C27	1.0UF 0402 X5R 6.3V	GRM15 Series Chip Monolithic Ceramic Capacitor
L1	3.3UH 1008 20% LQM2H	Murata LQM2HPN3R3MG0 Monolithic Type Chip Coil
L2	4N7 0402 0.1NH LQP15M	Murata Film Type Chip Coil
L3	0402	No Mount
P2	MM8430-2610	Murata Coax Connector
R3	0R 0402	Chip resistor 0.063W
R6	0R 0402	Chip resistor 0.063W
R10	0R 0402	Chip resistor 0.063W
R27	0R 0402	Chip resistor 0.063W
R28	0R 0402	Chip resistor 0.063W
S1	EMC SHIELD BOX	
U1	HDG200 MODULE R2A	H&D Wireless WiFi SIP
U2	LM809M3-2.63 SOT23	National Microprocessor reset circuit
X1	ALA931C5	Amotech chip antenna

5 Power Management

The HDG200 has an integrated Step Down (buck) DC/DC regulator for generating the intermediate digital supply voltage for the entire HDG200. This voltage internally supplies a number of on chip LDOs for various digital domains of HDG200. The DC/DC requires an external 3.3µH inductor and a capacitor of minimum 2.2uF, preferably 4.7uF.

The DC/DC uses PWM modulation for high load currents with an efficiency of better than 88% over the load range for the Transmit- and Receive modes.

For light load conditions such as idle mode, the DC/DC operates in PFM modulation with a lowered output voltage, ensuring the lowest current consumption while still maintaining the RAM content.

The DC/DC uses a soft-start sequence to prevent current spikes on the battery during power-up.

The DC/DC can be turned OFF by a command from Host when inductor L1 is not mounted. VDD_DCDC should then be supplied by an external source.

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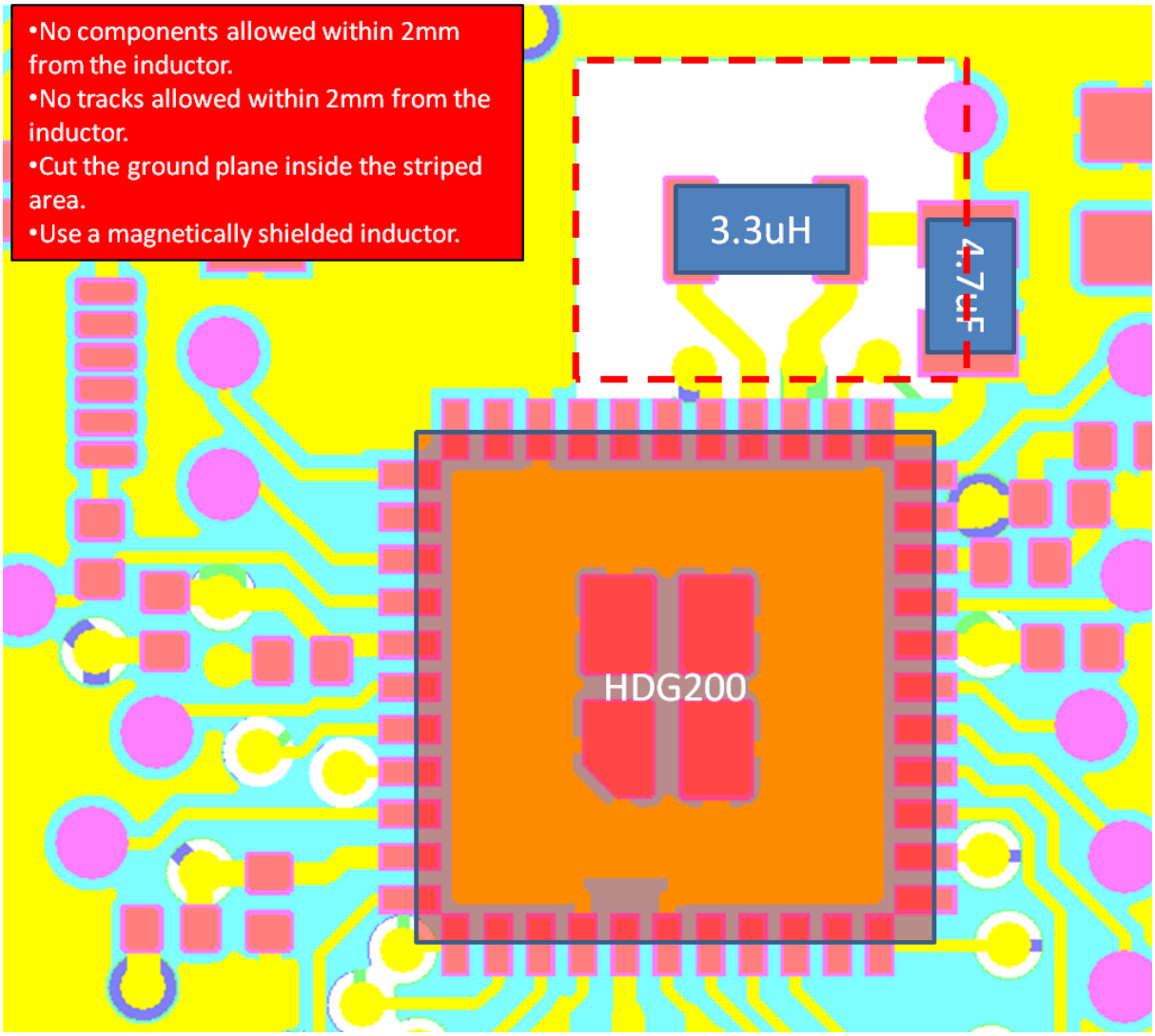
5.1 PCB layout example

In order to minimize the risk for crosstalk to other parts of the chip, it is extremely important that the PCB guidelines are followed. Below figure gives some more details PCB guidelines.



5.2 EMC Shield

To ensure that EMC/EMI requirements are met it is recommended that the HDG200 is covers by an EMC shield. It is recommended to include the DCDC inductor and decoupling capacitors under the shield to keep them as close to their respective pin as possible.

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6 Package Specifications

6.1 Mechanical outline QFN 44 pin

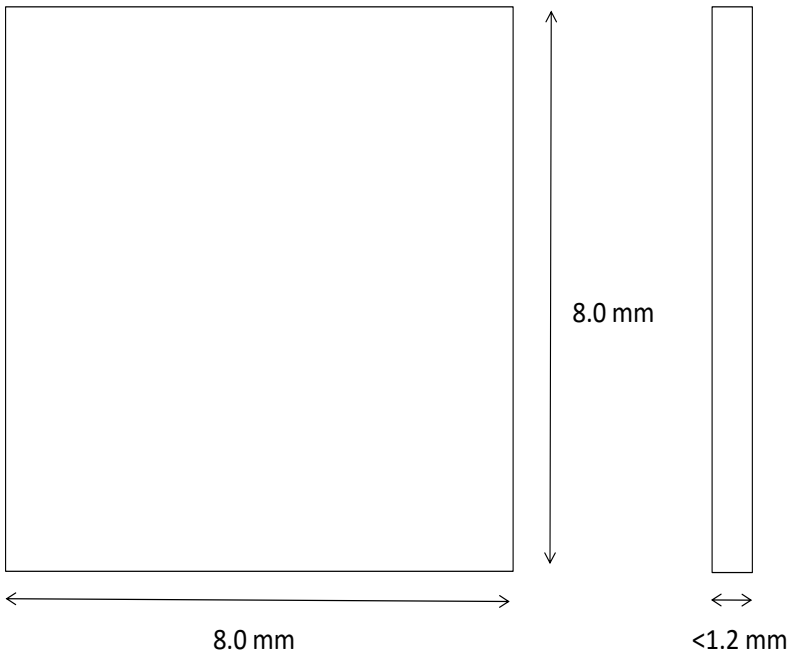

Figure 6-1: Mechanical drawing, 44 pin Quad Flat No-Lead (QFN) package.

Package specifications

6.2 Marking HDG200 QFN

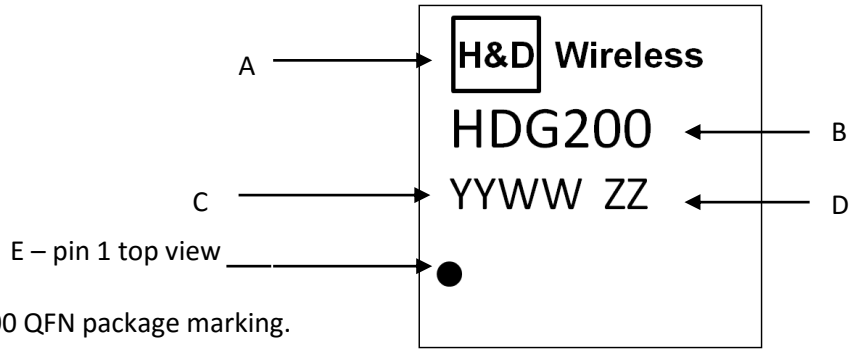

Figure 5-4: HDG200 QFN package marking.

Ref	Marking	Description
A	H&D Wireless	Company Logo
B	HDG200	Product name
C	YYWW	Production date. YY= year, WW=week
D	ZZ	Production lot
E	Square	Defines pin 1 (Top view)

Table 6-1: QFN package marking description

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6.3 Package pad dimension

HDG200 pad placement and sizes, top view. Units in mm.

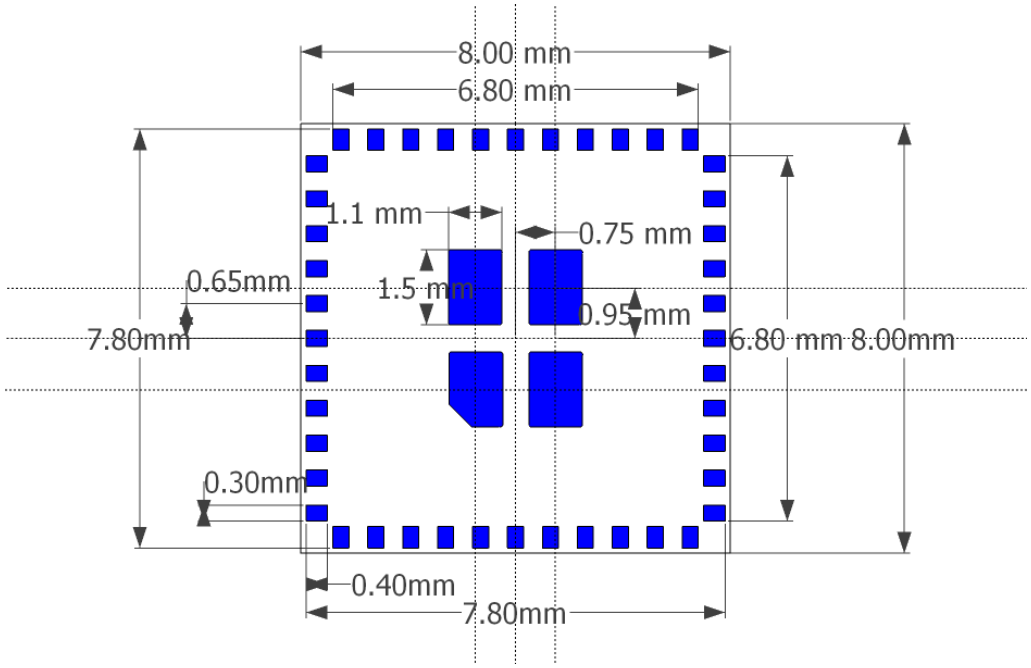

Figure 5.5: HDG200 Pad pattern, top view, units in mm

6.4 Mounting information

Recommended land pattern on the PCB

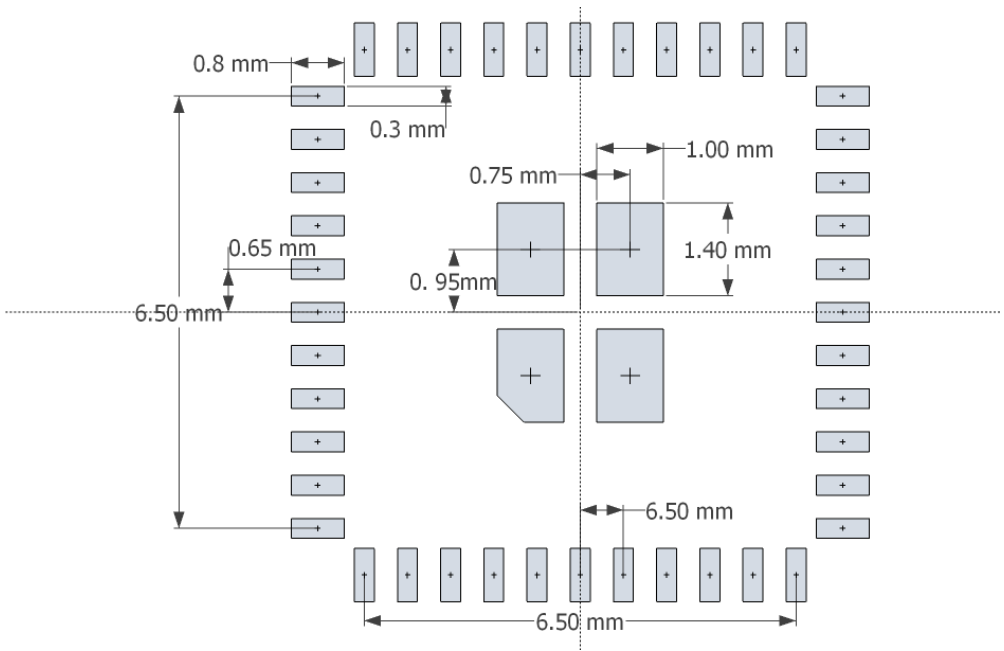

Figure 5.6: Recommended land pattern on the PCB, top view

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7 PCB Stackup

		Thickness um	
Top Layer		35	+5/-10
FR4	Core 16mil 1/1 oz 7628X2	260	+/-40
Ground plane		35	+5/-10
FR4	P.P 1506x1	740	+/-30
Power Plane		35	+5/-10
FR4	Core 16mil 1/1 oz 7628X2	260	+/-40
Bottom Layer		35	+5/-10
		1400	Tot

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