Hardware Design Guide
HDG229
Application Note

1 Preface

This document provides hardware design guidelines for the HDG229 module.

2 Introduction

2.1 Overview

HDG229 is a complete WLAN/BT System-in-Package module with EMC shield, ready for onboard integration in a hosted environment. HDG229 enables a cost efficient low power, high performance and feature rich client solution. It provides up to 150 Mbit/s data rate when operating in the OFDM mode and up to 11 Mbit/s data rate when operating in the DSSS/CCK mode.

HDG229 integrates RF, baseband/MAC, Bluetooth Package Engine, memory, RF filters, oscillator and EMC shield into a highly integrated and optimized module solution with high quality and reliability to a complete standalone solution with only a few external components.

This highly integrated solution is optimized for customer applications running on a Linux host. The host interface supports SDIO 3.0. Internal RAM comprises both code and data memory eliminating the need for external RAM, Flash or ROM memory interfaces. MAC address, trimming values etc. are stored in the on-board memory.

2.2 Key Features

- Support for 802.11a/b/g/n.
- Data Rates: 20MHz channel bandwidth: 1-72Mbps; 40MHz channel bandwidth: 13-150Mbps.
- Modulation: BPSK, CCK, QPSK, 16QAM, 64QAM for WLAN and GFSK/π/4DQPSK/8DPSK/LE for Bluetooth.
- Open, WEP and WPA/WPA2 encryption.
- Few external components.
- Low power consumption due to efficient PA design and power off mode.
- Supports Bluetooth-WLAN coexistence.
- Extensive DMA hardware support for data flow to reduce CPU load.
- Advanced power management for optimum power consumption at varying load.
- External interfaces: 4 bit SDIO 3.0 for WLAN/Bluetooth, optional UART for Bluetooth only.
- On-board High Frequency High Precision Oscillator.
- Small footprint 8 x 8 mm 42-pin LGA package.
- RoHS Compliant.

3 Block Diagram

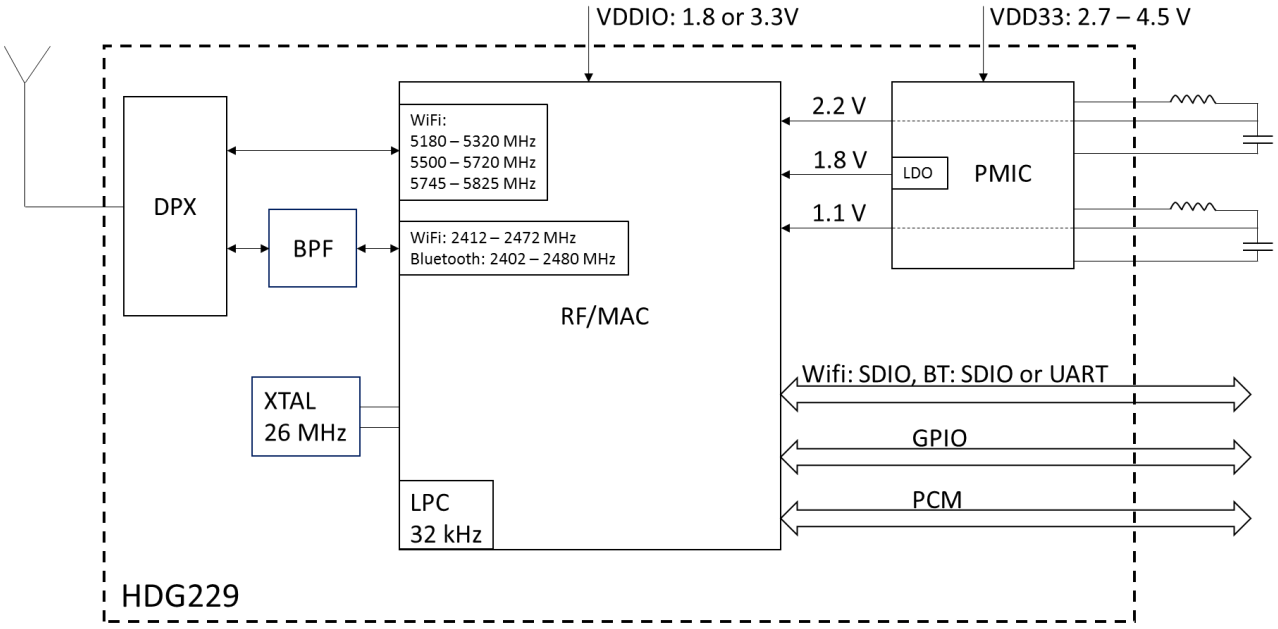

Figure 1. Block diagram.

4 Reference schematic

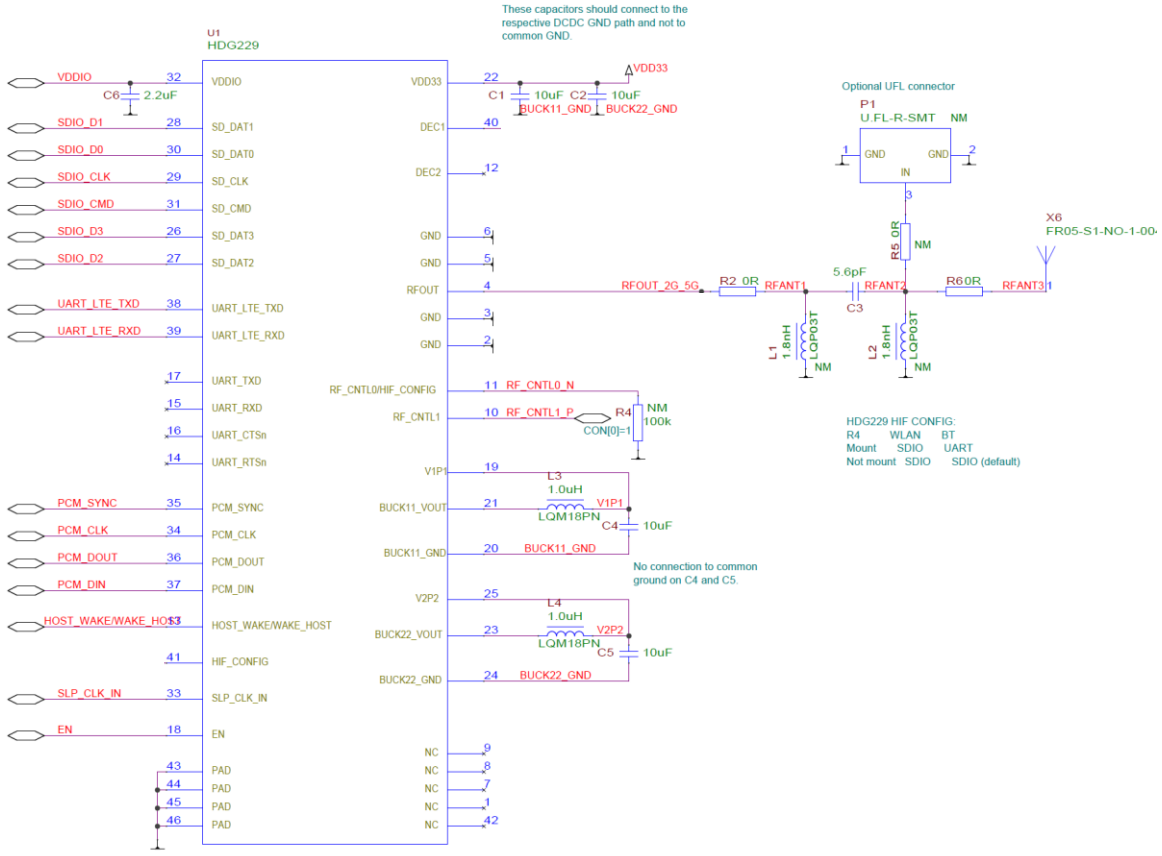

Figure 2. HDG229 reference schematic.

The output is selectable to go either to an UF.L connector or a chip antenna. The selection is done by either mounting resistor R5 or R6. The impedance matching for the antenna is dependent on any mechanical objects near the antenna and should be tuned for each design.

5 Pin Description

The HDG229 module provides the following pins.

Table 1. RF Interface

Module Pin number	Pin Name	Description
4	RFOUT	RF input/output

Table 2. SDIO Host Interface (for WLAN or WLAN/Bluetooth depending on HIF config)

Module Pin number	Pin Name	Description
26	SD_DAT3	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used
27	SD_DAT2	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
28	SD_DAT1	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt
29	SD_CLK	Clock input
30	SD_DAT0	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line
31	SD_CMD	SDIO 4-bit mode: Command SDIO 1-bit mode: Command

The SDIO Interface supports 1-bit and 4-bit SDIO transfer modes up to 100MHz clock frequency.

Table 3. PCM Interface

Module Pin number	Pin Name	Description
34	PCM_CLK	PCM Clock signal.
35	PCM_SYNC	PCM Sync pulse signal.
36	PCM_DOUT	PCM Data
37	PCM_DIN	PCM Data.

Table 4. UART Interface (for Bluetooth depending on HIF config)

Module Pin number	Pin Name	Description
14	UART_RTSn	Request To Send, active low.
15	UART_RXD	Serial Data.
16	UART_CTSn	Clear To Send, active low.
17	UART_TXD	Serial Data.

The UART interface supports baud rates from 1.2kB/s up to 4MB/s.

Table 5. LTE Coex Interface

Module Pin number	Pin Name	Description
38	UART_LTE_TXD	TX Serial Data.
39	UART_LTE_RXD	RX Serial Data.

Table 6. General

Module Pin number	Pin Name	Description
1	NC	No Connect, leave open.
7	NC	No Connect, leave open.
8	NC	No Connect, leave open.
9	NC	No Connect, leave open.
10	RF_CNTL1	For antenna diversity/FEM control if used.
11	RF_CNTL0/HIF_CONFIG	For antenna diversity/FEM control if used. For host config setup, see table below.
12	NC	No Connect, leave open.
13	HOST_WAKE/WAKE_HOST	Can be configured as a wake signal.
18	EN	Enable.
33	SLP_CLK_IN	Entry point for external low frequency clock.
40	NC	No connect, leave open.
41	HIF_CONFIG	For compatibility with HDG226, place a 100k resistor to ground, not mounted.
42	NC	No connect, leave open.

Table 7. Ground and Supply

Module Pin number	Pin Name	Description
2	GND	Ground.
3	GND	Ground.
5	GND	Ground.
6	GND	Ground.
19	V1P1	1.1V feedback from external LC filter.
20	BUCK11_GND	Ground for 1.1V DCDC-regulator, see schematic and layout for comments.
21	BUCK11_VOUT	1.1V DCDC regulator output, connect to external LC filter. See schematic and layout for comments.
22	VDD33	Connect to 3.3V supply.
23	BUCK22_VOUT	2.2V DCDC regulator output, connect to external LC filter. See schematic and layout for comments.
24	BUCK22_GND	Ground for 2.2V DCDC-regulator, see schematic and layout for comments.
25	V2P2	2.2V feedback from external LC filter.
32	VDDIO	Digital IO supply, can be connected to VDD33 and share decoupling if both VDDIO and VDD33 have the same voltage.
43	GND	Ground pad.
44	GND	Ground pad.
45	GND	Ground pad.
46	GND	Ground pad.

6 Host Interface Configuration

The HDG229 can be configured to use either SDIO for both WLAN and BT, or SDIO for WLAN and UART for BT according to the following table. Following reset, the status of RF_CNTL0 will be checked and host interface set accordingly. After this, the RF_CNTL0 will resume its normal function.

Table 8. HIF Configuration

R4	WLAN	BT/BLE
Mount	SDIO	UART
Not Mount (default)	SDIO	SDIO

7 Bill of Material

Table 9. SPB229 reference design BOM

Comp	Part name	MFG nr.	Description
U1	HDG229		HDG229 PCB Module
C1, C2, C4, C5	10UF 0603 X6S 16V 20%	GRM188C81C106MA73	Murata ceramic chip capacitor
C3	5.6PF 0201 C0G 0.25PF 50V	GRM0335C1H5R6CA01	Murata ceramic chip capacitor
C6	2.2UF 0402 X6S 6.3V 20%	GRM155C80J225ME95	Murata ceramic chip capacitor
L1, L2	TBD		
L3, L4	1.0UH 0603 LQM18PN	LQM18PN1R0NF0	Murata LQM18 coil
R2, R6	0R 0201	ERJ-1GE0R00C	Panasonic chip resistor 1/20 W
X6	Ceramic Antenna SMD	FR05-S1-NO-1-004	Fractus dual-band antenna
		or	
P1	U.FL-R-SMT-1	CL331-0471-2-xx	Hirose U.FL RF Connector

The values of L1, L2 and C3 should be verified in final design including mechanics.
If connector P1 is used instead of antenna X1, R5 shall be mounted instead of R6.

8 PCB layout

This section describes the layout for the SPB229 module that is the reference design for HDG229.

FCC and IC will certify HDG229 as a modular transmitter. To comply with these approvals, it is vital to follow the instructions below in detail, especially for the RF traces. It is acceptable to use either U.FL connector with approved antenna or the approved chip antenna.

Include a pi-network in front of the antenna to add the possibility to tune its impedance to 50ohm. The module requires a 50 ohm load on its RF pin. If different antenna is used, the matching components need to be revised.

The four layers of the reference pcb is shown below, where the pink trace is the VDD33 net, the green is the V1P1 (1.1V) and V2P2 (2.2V) DCDC voltages and the black is BUCK11_GND and BUCK22_GND (DCDC GND). Note that the black net it also routed on layer 3. The decoupling capacitors are placed close to the module. See 8.1 for more details regarding the layout of the DCDC outputs.

The trace width of the RF line is 0.2 mm and the total length is 12 mm. For PCB stack-up, se section 9.

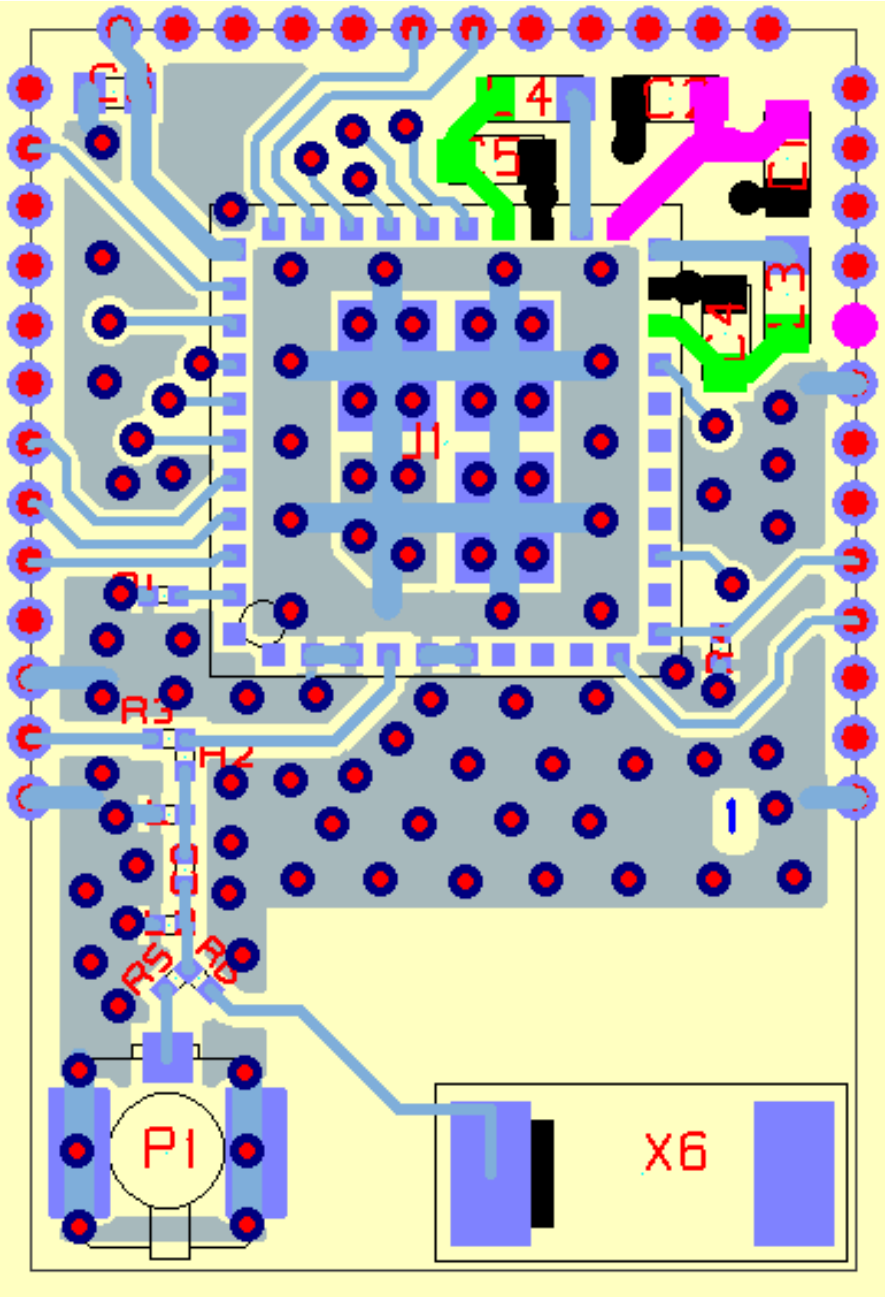

Figure 3. Top layer.

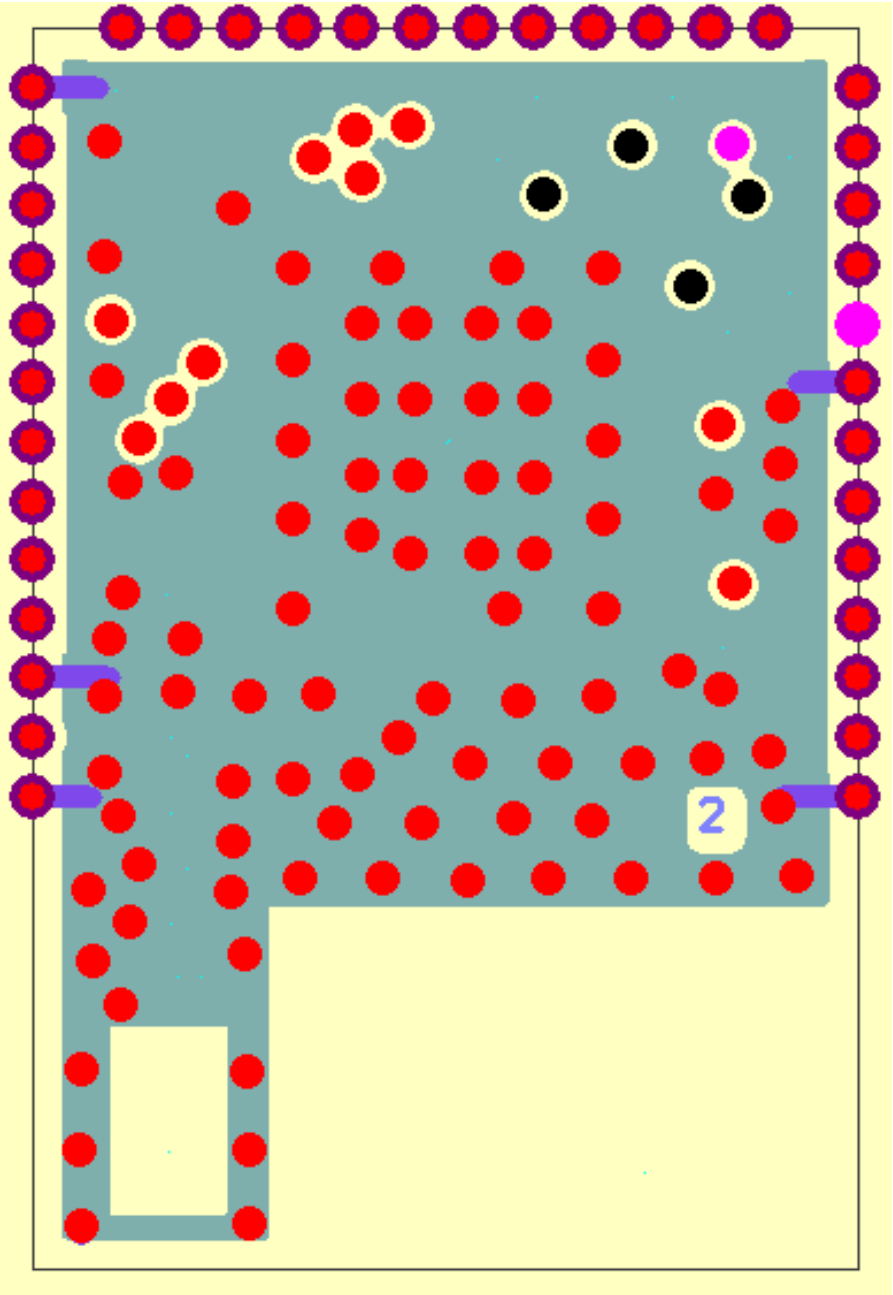

Figure 4. Second layer (RF ground).

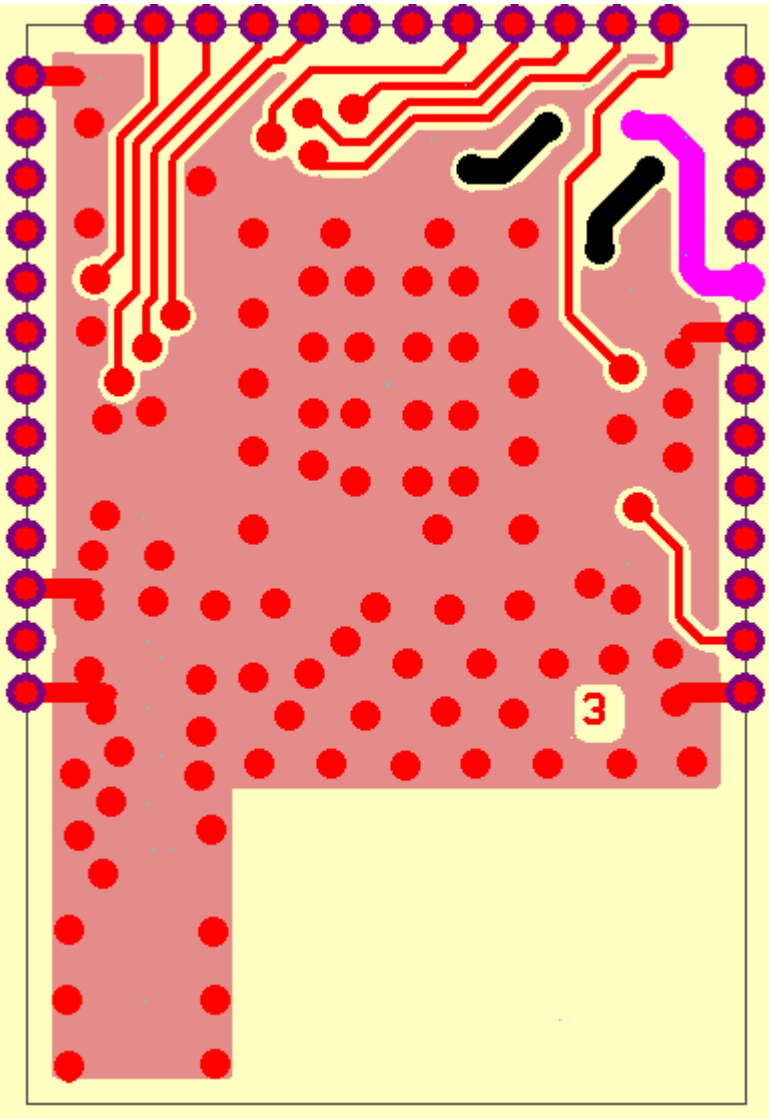

Figure 5. Third layer, ground and routing.

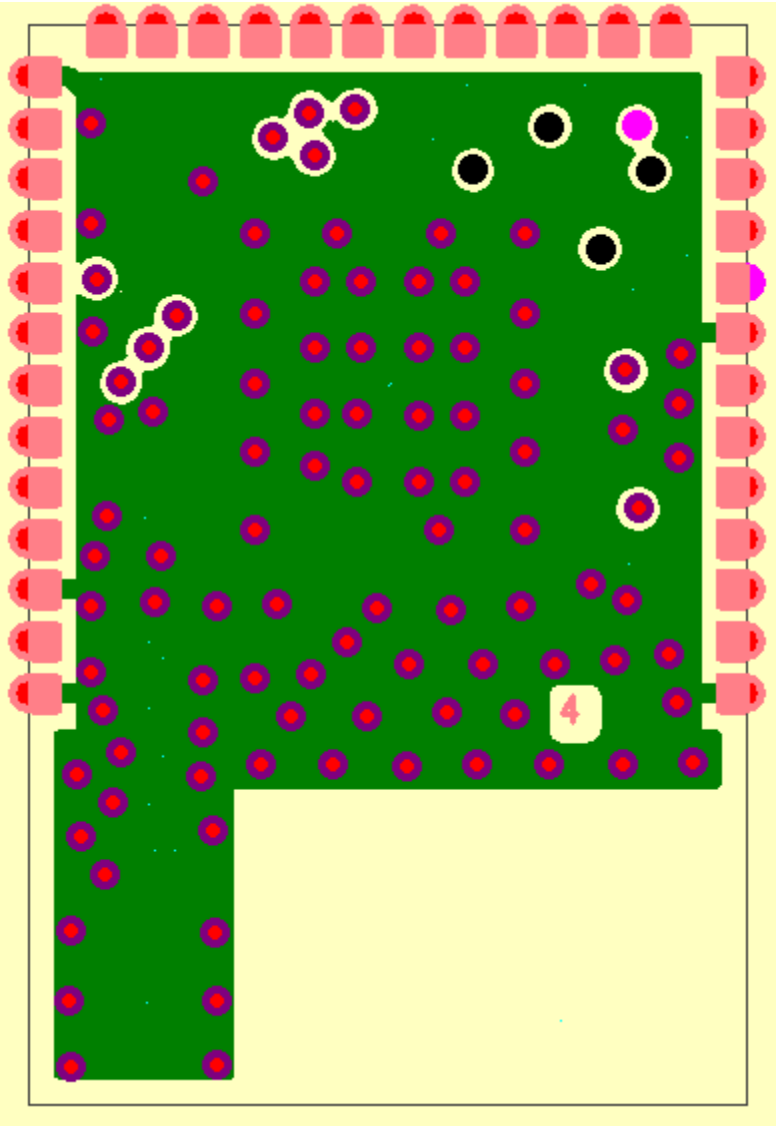

Figure 6. Bottom layer, ground.

8.1 Layout of the DCDC circuitry

The DCDC parts of the module requires some special attention. L3/C4 and L4/C5 are placed so that the respective capacitor ground returns are fed back to the DCDC ground pins of the module without connecting to the common ground.

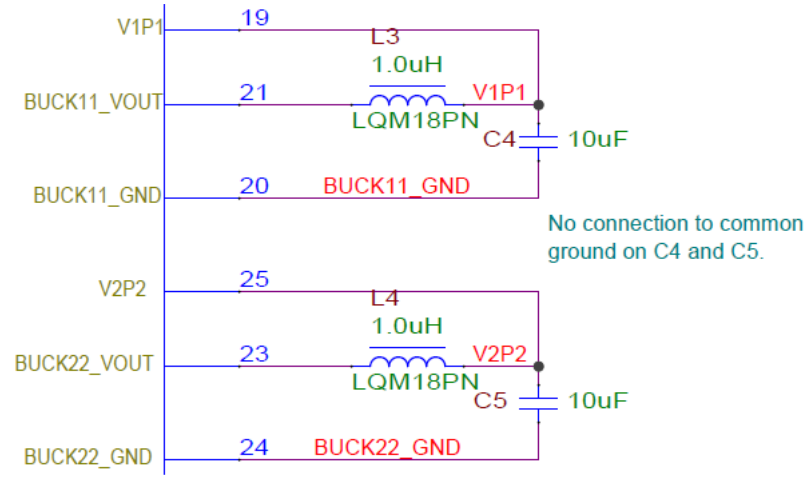

Figure 7. Schematic of the DCDC components.

VDD33 is fed to pin 22 of the module as well as the two decoupling capacitors C1/C2. The ground points of these capacitors are also connected to the respective DCDC ground pins of the module through a connection on layer 3.

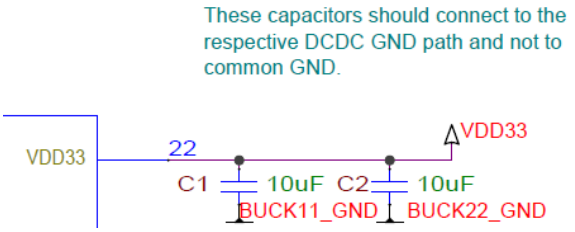

Figure 8. Schematic of the VDD33 decoupling capacitors.

9 Reference PCB Stack-up

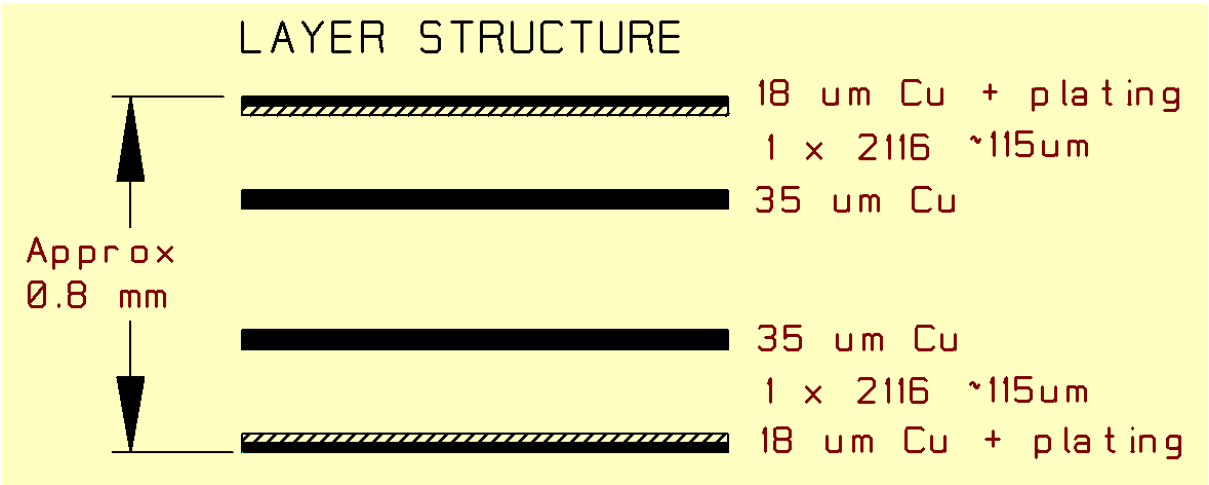

Figure 9. Reference PCB stack-up

10 RF connection/antenna

The surface mounted antenna used in the reference design is the dual band antenna FR05-S1-NO-1-004 from Fractus. It has a peak gain of 1.8dB dBi in the 2.4-2.5GHz band and 4.9dBi in the 4.9-5.875GHz band. The HDG229 module will be FCC/ETSI certified with this antenna. Make sure that the layout follows the recommendations in this guideline so the antenna gain and path loss will not differ from the reference design. It is always good practice to add pads for a pi-network close to the antenna if it needs to be tuned.

The product may also be approved with an external balanced flex antenna with a cable connected to the U.FL connector.

Antenna	Max Gain 2.4 GHz	Max Gain 5 GHz	Power Table (see Table 11 below)	Reference Design Mounting Option (see Table 12 below)
Fractus FR05-S1-NO-1-004	1.8 dBi	4.9 dBi	V1	1
TBD (i.e. Molex 146153-0100)	3.0 dBi	4.5 dBi	V1	2

Table 10. List of FCC approved antennas.

	2.4 GHz				5 GHz			
Power Table	Max power level 11bg	Max power level 11n	Max power level ch 1 FCC	Max power level ch 11 FCC	Max power level BT/BLE	Max power level 11a	Max power level 11n, HT20	Max power level 11n, HT40
V1	16	15	11b: TBD 11g: TBD 11n: TBD	11b: TBD 11g: TBD 11n: TBD	6	16	15	14

Table 11.List of power tables for the approved antennas (refer to previous table).

The customer will need to sign a Software Configuration Control Agreement declaring the integration responsibility of the HDG229 WLAN/BT product when it comes to making sure compliance to regulatory domain.

The different mounting options are summarized in below table.

Comp	Using the Fractus antenna Mounting Option 1	Using the U.FL connector Mounting Option 2
C3	TBD	5.6PF 0201 C0G 0.25PF 50V
L1	TBD	Not Mounted
L2	TBD	Not Mounted
R5	0R 0201	Not Mounted
R6	Not Mounted	0R 0201
X6	FR05-S1-NO-1-004	Not Mounted
P1	Not Mounted	U.FL-R-SMT

Table 12. Mounting options.

11 Layout consideration for chip antenna

Note that there should be no PCB under the antenna part if the HDG229 + antenna is mounted as below picture.

[Picture to be replaced]

Figure 10. HDG229 reference design mounted on a mother board.

Also, note that no objects, metal or non-metal, should be closer than 10 mm from the antenna. Make also sure that there is no metal in the casing that will interfere with the radiation pattern.

12 Package

For package specification, mechanical outline and mounting information, please refer to the datasheet.

13 Notes

H&D Wireless retains the right to change this document at any time, without prior notice. HDW makes no warrantees regarding the information in this document. If in any doubt, please consult with your TCB regarding the recommendations and information in this document.

14 Revision History

Rev	Date	Description
A	20170206	First draft
B	20170221	Updated package footprint
C	20170912	Updated for new reference disign