Hardware Design Guide
SPB209A
Application Note

1 Preface

This document provides hardware design guidelines for the SPB209A module.

2 Introduction

2.1 Overview

SPB209A is a complete WLAN/BT/NFC module with EMC shield, ready for onboard integration in a hosted environment. SPB209A enables a cost efficient ultra-low power, high performance and feature rich client solution. It provides up to 433 Mbit/s data rate when operating in the OFDM mode and up to 11 Mbit/s data rate when operating in the DSSS/CCK mode.

SPB209A integrates RF, baseband/MAC, Bluetooth Package Engine, NFC, memory, RF filters, oscillator, antenna (option) and EMC shield into a highly integrated and optimized module solution with high quality and reliability to a complete standalone solution with no need for external components.

This highly integrated solution is optimized for customer applications running on a Linux host.
The host interface supports SDIO 3.0, High Speed UART and I2C. Internal RAM comprises both code and data memory eliminating the need for external RAM, Flash or ROM memory interfaces. MAC address, trimming values etc. are stored in the on board memory.

2.2 Key Features

- Support for 802.11a/b/g/n/ac
- Data Rates: 20MHz channel bandwidth: 1-86Mbps; 40MHz channel bandwidth: 13-200Mbps; 80MHz channel bandwidth: 29-433Mbps
- Modulation: BPSK, CCK, QPSK, 16QAM, 64QAM 256 QAM for WLAN and GFSK/π/4DQPSK/8DPSK/LE for BT
- Open WEP, WPA/WPA2 encryption
- No external components except for the antenna options
- Low power consumption due to efficient PA design and power off mode
- An on-board 32 kHz oscillator maintains real time in power save mode, allows the high frequency clock to be turned off.
- Supports BT-WLAN coexistence and ISM-LTE coexistence.
- Extensive DMA hardware support for data flow to reduce CPU load.
- Advanced power management for optimum power consumption at varying load.
- External interfaces 4 bit SDIO 3.0 for WLAN and UART/PCM for BT interface.
- On-board High Frequency High Precision Oscillator 37.4 MHz
- Small footprint 14 x 14 mm (196 mm2) 41-pin
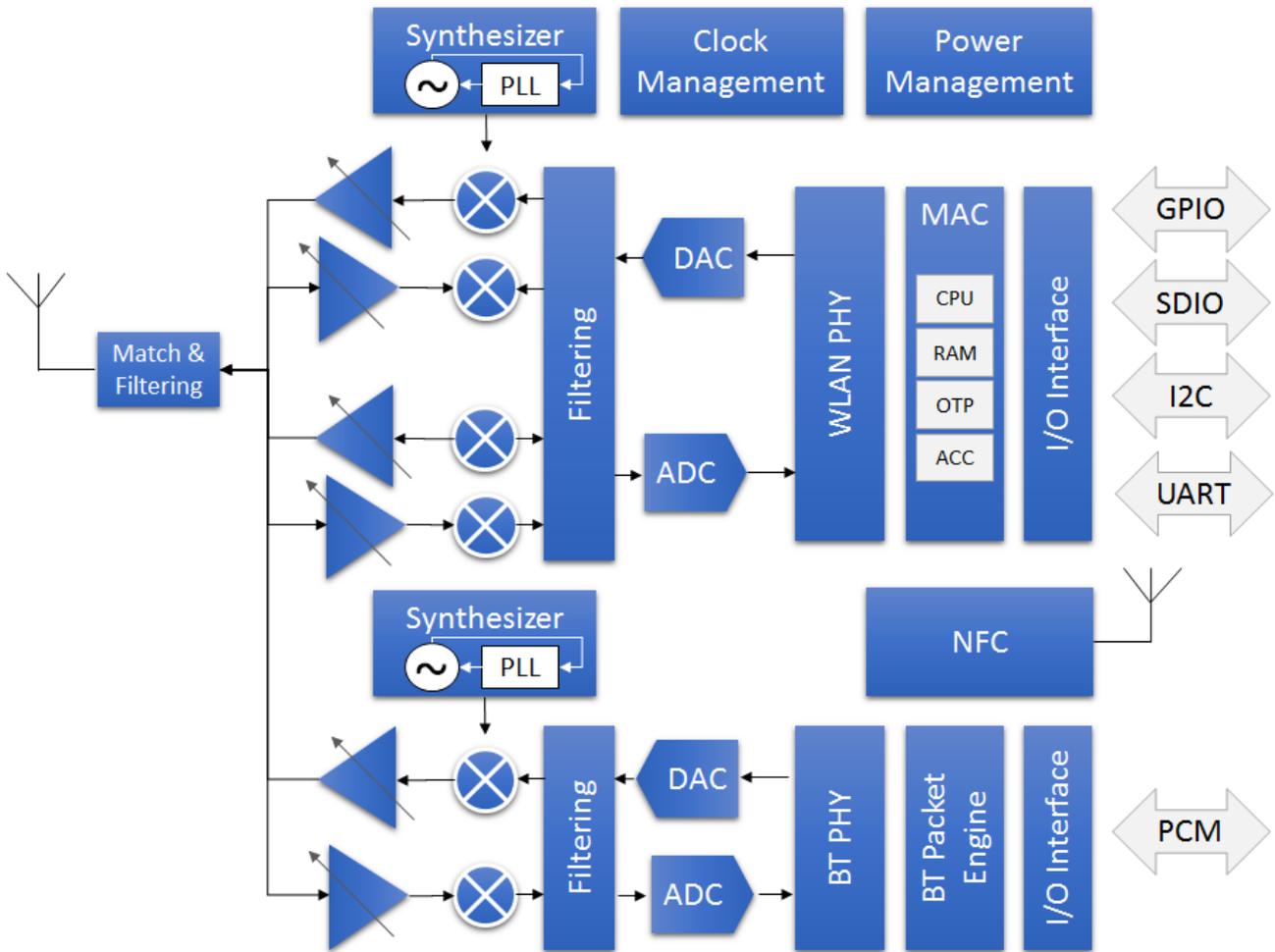
- RoHS Compliant

3 Block Diagram

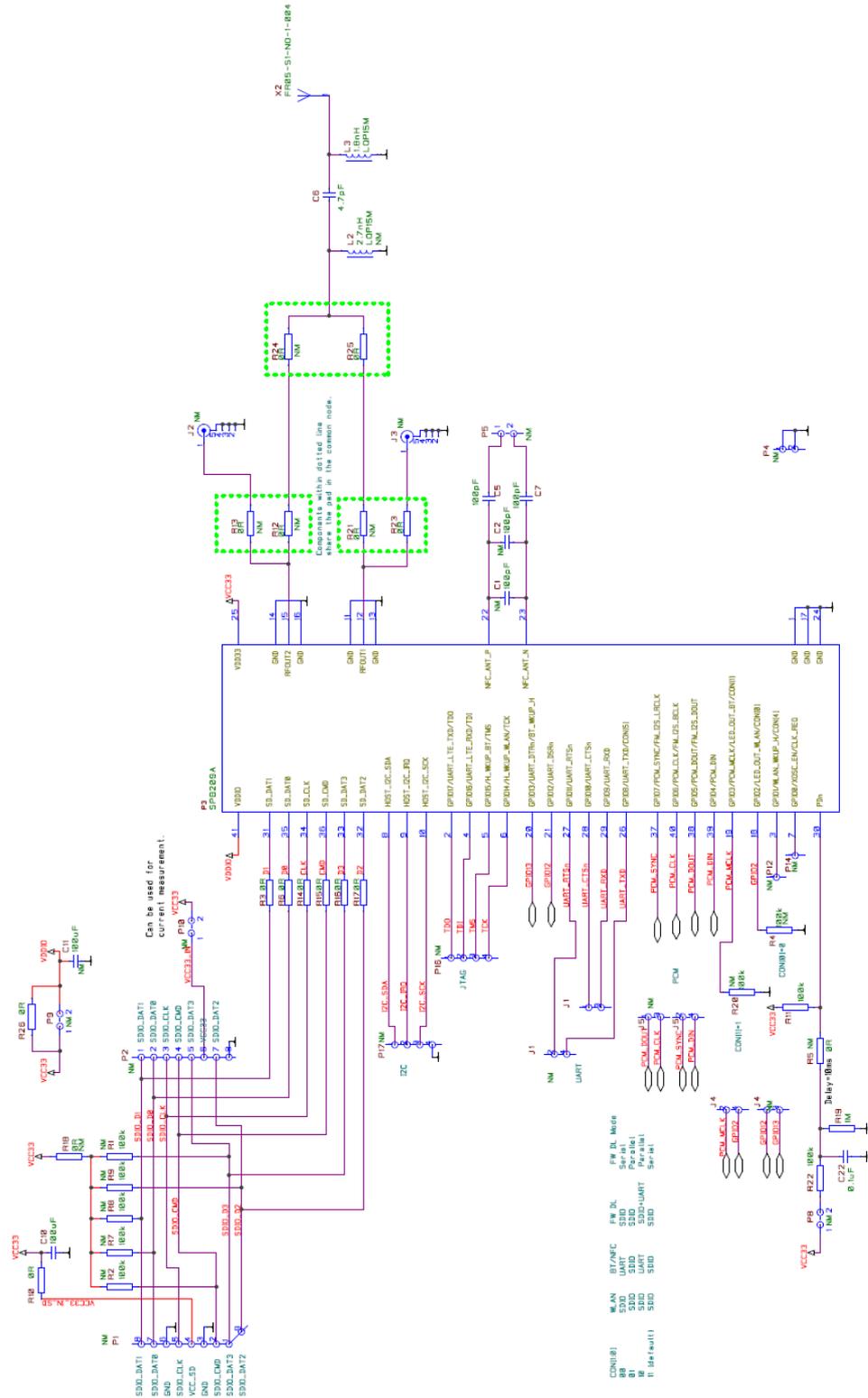*Figure 1. Block diagram.*

4   Reference schematic

Figure 2. SPB209A reference schematic.

Note that the module has two RF output options, and one of them is chosen depending on the version ordered. The reference schematic is made so both versions can be used and have access to the single common antenna by means of the 0R resistors on the output.

5   Bill of Material

Comp	Part name	MFG nr	Description
A1	PCB		Printed circuit board
C5	100PF 0402 C0G 50V 5%	GRM1555C1H101JA01D	Murata GRM15 Series Chip Monolithic Ceramic Capacitor
C6	4.7PF 0402 C0G 50V		Murata GRM15 Series Chip Monolithic Ceramic Capacitor
C7	100PF 0402 C0G 50V 5%	GRM1555C1H101JA01D	Murata GRM15 Series Chip Monolithic Ceramic Capacitor
C10	100UF 6.3V X7R 1206	GRM21BR61A106KE19L	Ceramic chip capacitor
C22	0.1UF 0402 X7R 16V 10%	GRM155R71C104KA88D	GRM15 Series Chip Monolithic Ceramic Capacitor
L3	1N8 0402 0.1NH LQP15M	LQP15MN1N8B02	Murata LQP15MN Film Type Chip Coil
P3	SPB209A		SPB209A PCB Module
P8	WAFER 2-2.54		Pin Posts single row C/C 2.54 2-Pin
R3	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
R6	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
R10	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
R11	100K 0402 1%	RC0402FR-07100KL	Chip resistor 0.063W
R14	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
R15	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
R16	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
R17	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
R19	1M 0402 1%	RC0402FR-071ML	Chip resistor 0.063W
R22	100K 0402 1%	RC0402FR-07100KL	Chip resistor 0.063W
R23	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
R25	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
R26	0R 0402	RC0402JR-070RL	Chip resistor 0.063W
X2	ANTENNA FR05-S1-NO-1-004 SMD	FR05-S1-NO-1-004	Fractus Dual-band Reach Xtend Chip Antenna

Figure 3. Reference schematic BOM.

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6   PCB layout

Use normal layout common sense. Include a pi-network in front of the antenna to add the possibility to tune its impedance to 50ohm. The module requires a 50ohm load on its RF pins. If another antenna is used, the matching components need to be revised. The power supply is arranged as power planes on the bottom layer with vias up to the top level. The four layers of the reference pcb is shown below, where the red area is the VCC33 net and the black is the VDDIO net.
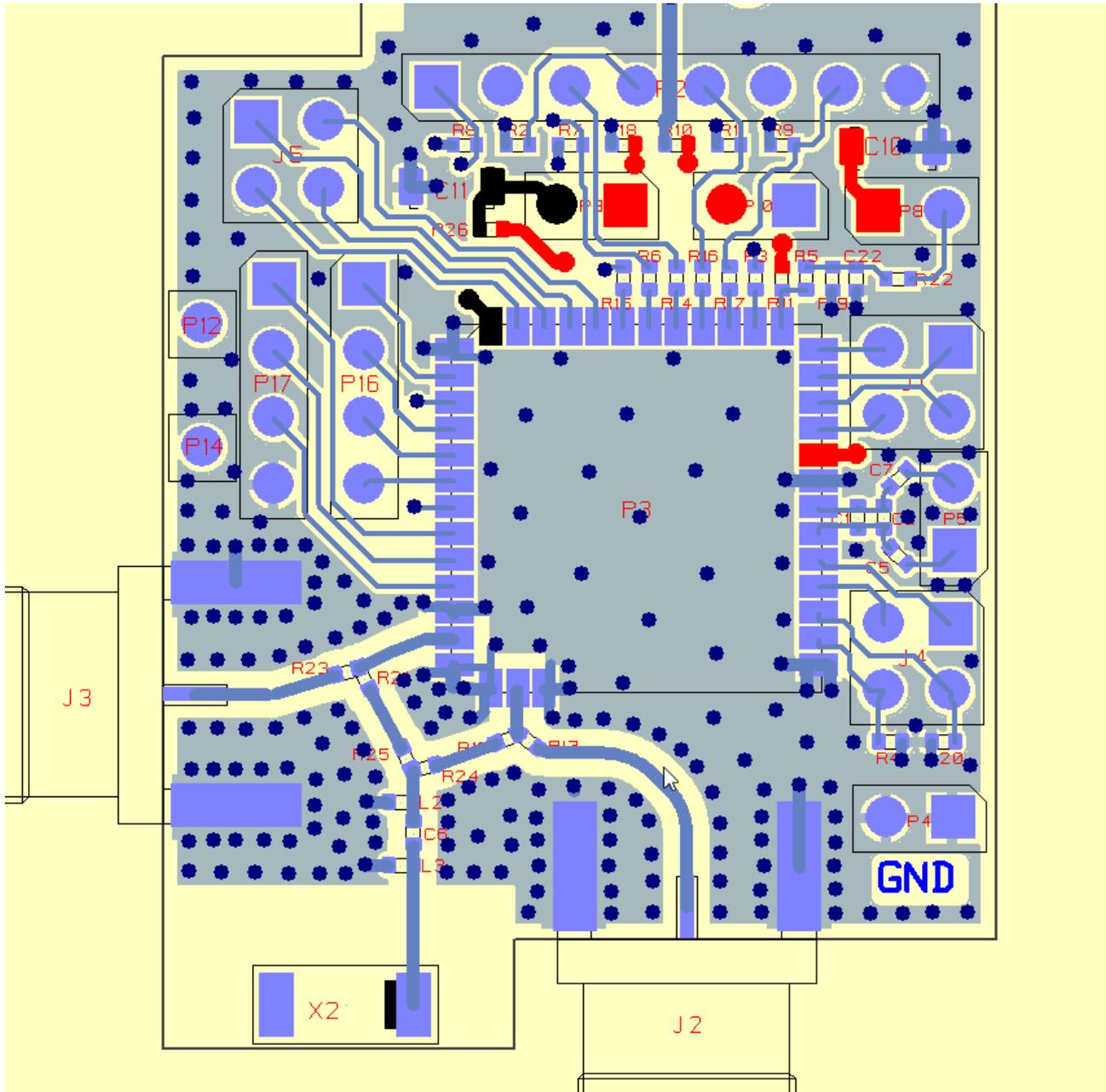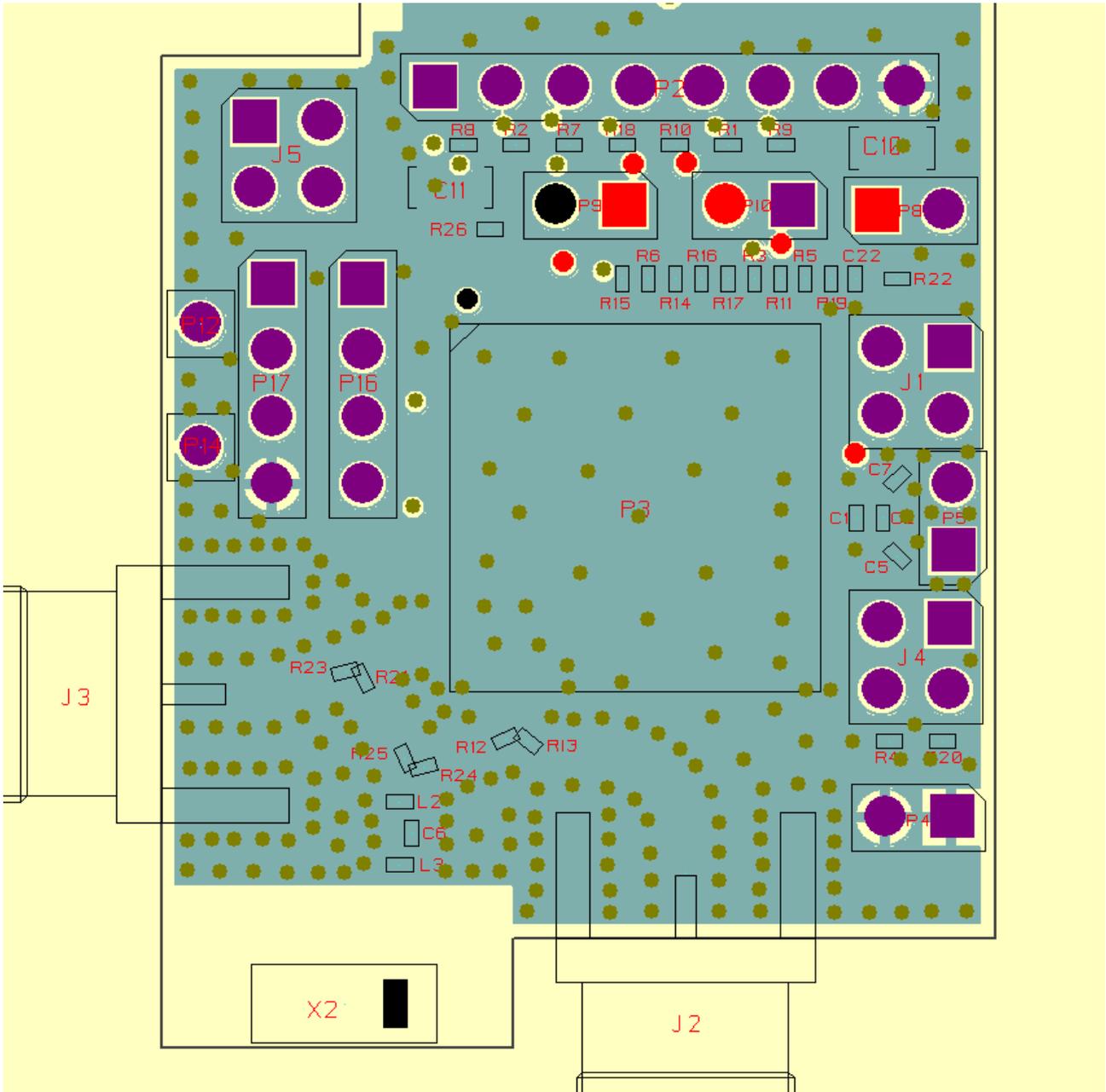

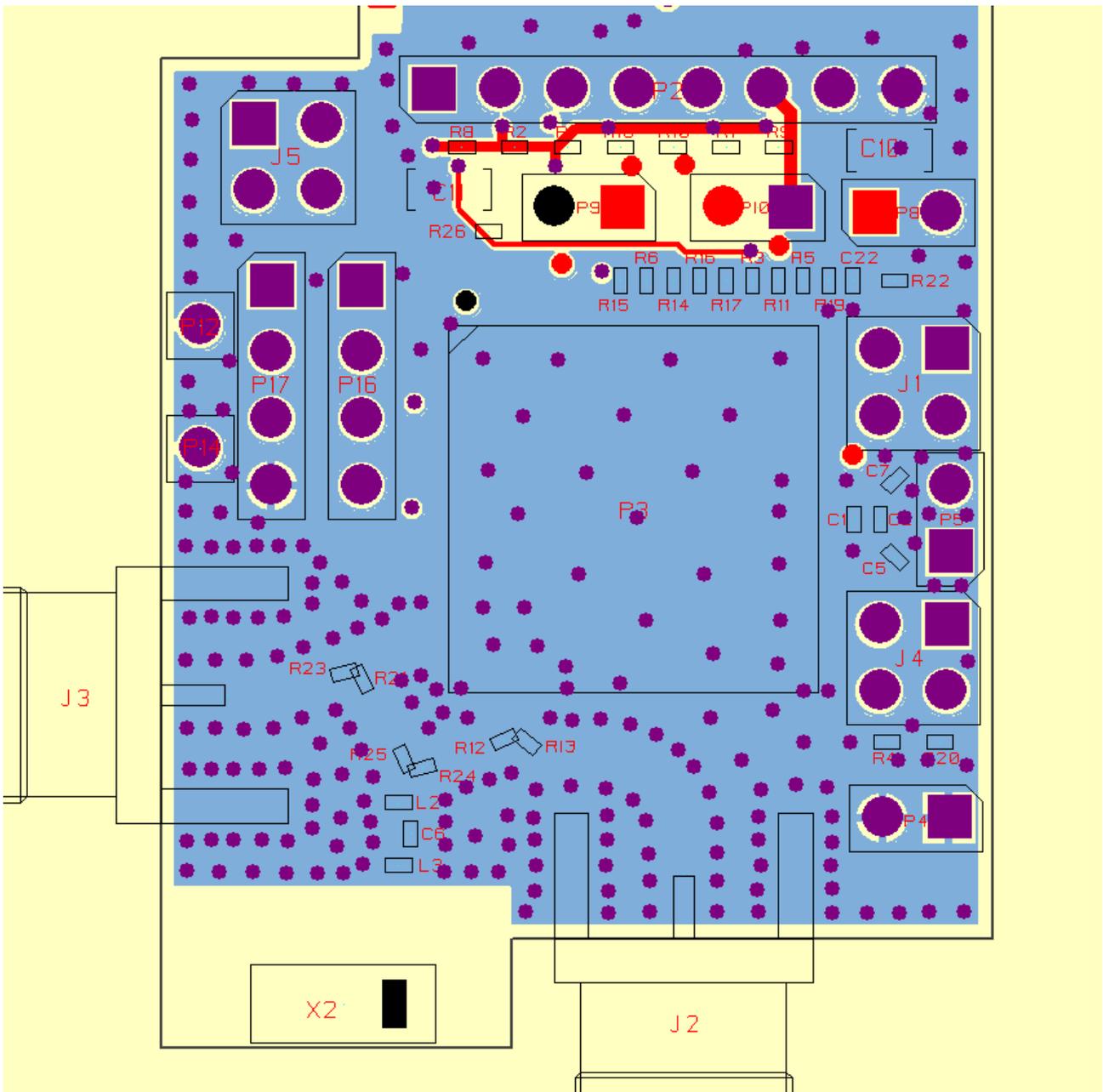*Figure 4. Top layer.*

Figure 5. Second layer (RF ground).

Figure 6. Third layer, ground and supply.
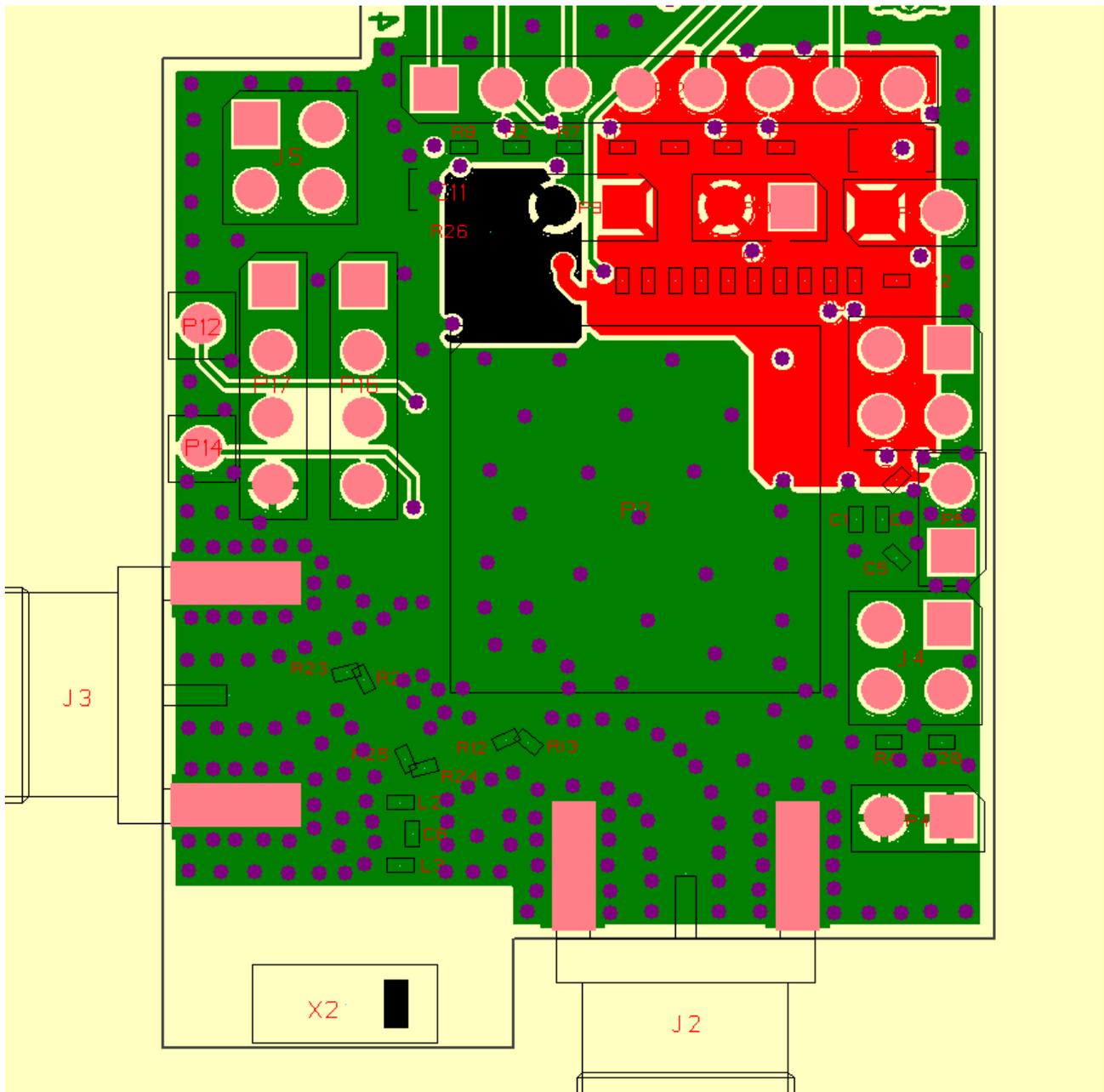
1453- SPB209A Hardware Design Guide

Figure 7. Bottom layer, ground and supply.

7   NFC

An NFC-antenna is not included in the reference design, but may be added as an external component. In that case the matching for the NFC antenna must be checked. This is not covered in this guide.

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8 Package Specifications

8.1 Mechanical outline
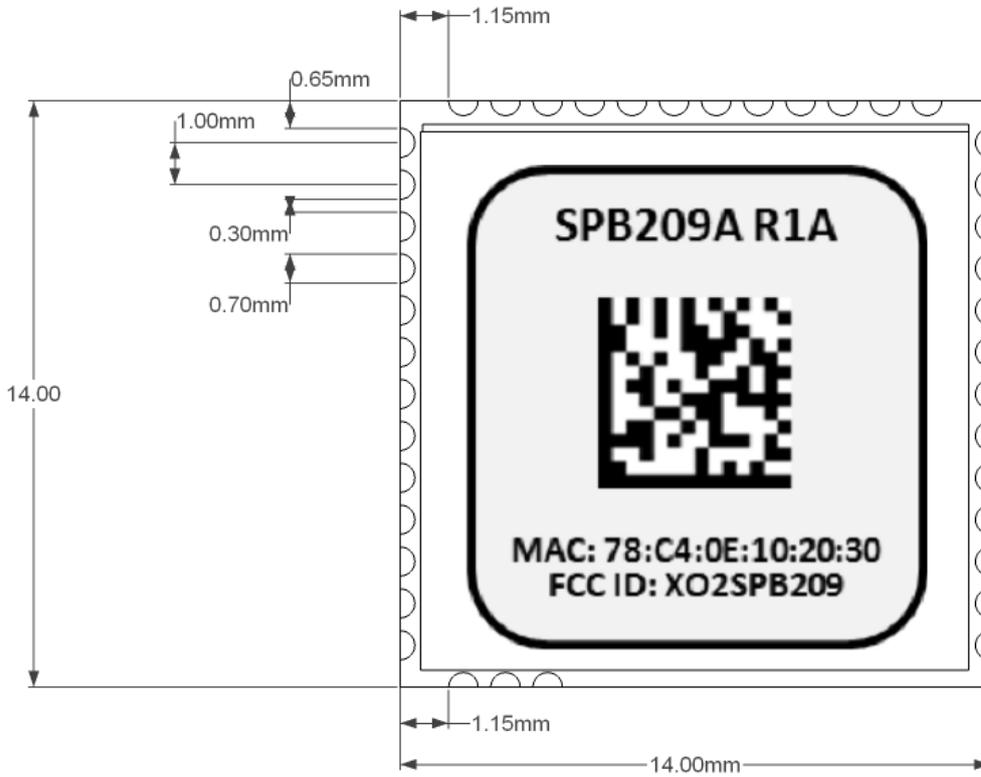
Figure 8. Package dimensions, top view.

Figure 9. Package dimensions, side view.

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8.2 Mounting information

Recommended land pattern on the PCB.
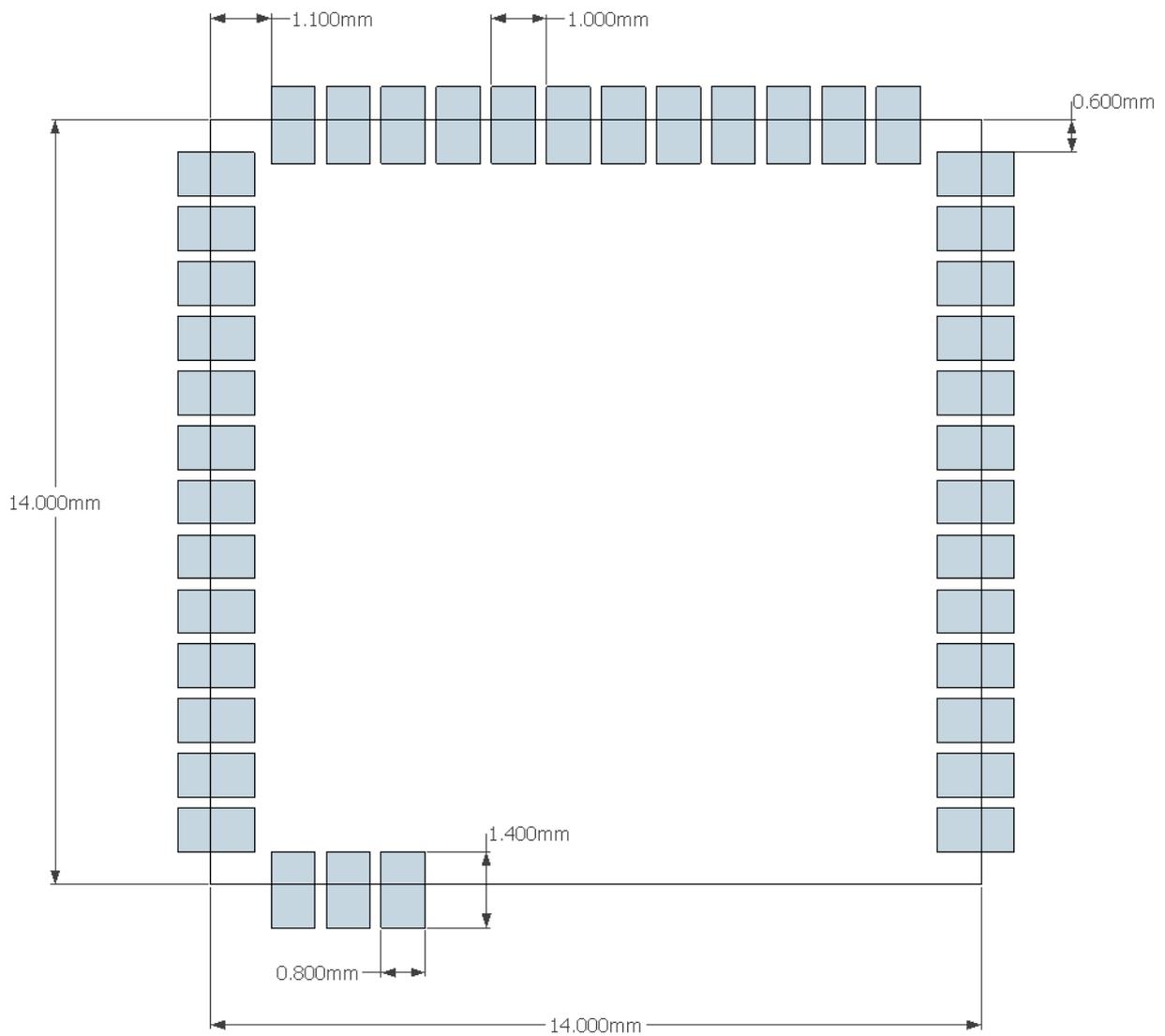
Figure 10. Recommended land pattern on the PCB, top view.

1453- SPB209A Hardware Design Guide

9   Reference PCB Stack-up

LAYER STRUCTURE

18 um Cu + plating

0.26 mm   1 x PP1080 + 1 x PP7628

35 um Cu
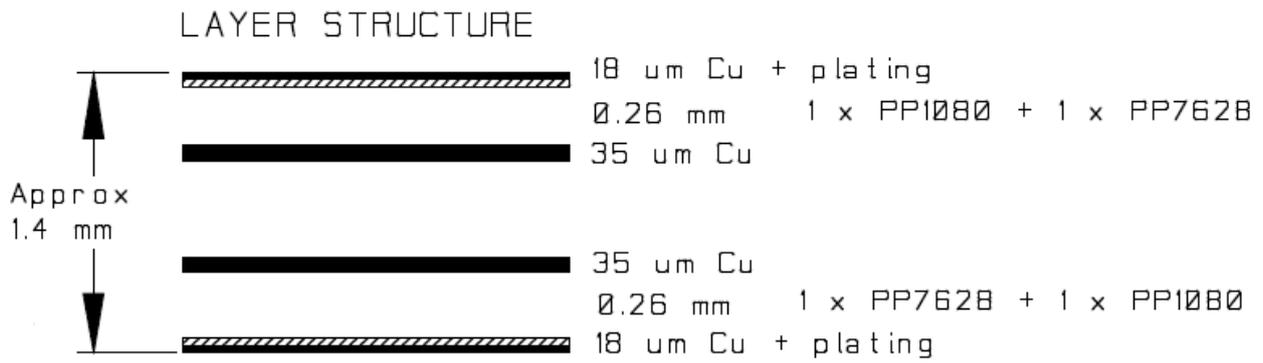
Approx
1.4 mm

35 um Cu

0.26 mm   1 x PP7628 + 1 x PP1080

18 um Cu + plating

Figure 11. Reference PCB stack-up.

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